Effects of high-temperature anneals and ^{60}Co gamma-ray irradiation on strained silicon on insulator

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Strained silicon on insulator was exposed to high-temperature annealing and high-dose ^{60}Co gamma (γ)-ray irradiation to study the tenacity of the bond between the strained Si film and the underlying buried oxide. During the high-temperature anneals, the samples were ramped at a rate of 150°C/s to 850°C then ramped to 1200, 1250, and 1300 °C at a rate of approximately 5×10^5 °C/s for millisecond duration anneals. For the irradiation experiments, the samples were irradiated with ^{60}Co γ rays to a dose of 51.5 kGy. All samples were characterized by ultraviolet (UV) Raman, pseudo metal-oxide-semiconductor field-effect transistor (Ψ-MOSFET) current voltage, Hall mobility, and photoluminescence (PL) to verify changes in strain. UV Raman, PL, and Ψ-MOSFET measurements show no strain relaxation for the high-temperature annealed samples and only very slight relaxation for the γ-ray irradiated samples. © *2007 American Institute of Physics*.
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INTRODUCTION

Since strained silicon on insulator (sSOI) structures take advantage of both SOI and strain-enhanced metal oxide semiconductor field effect transistor (MOSFET) carrier mobility, sSOI is considered as one of the most prominent material candidates for high-performance, low-power MOSFETs.[1–4] In previous studies, the stability of the strain with thermal processing[5–7] and nanopatterning[8–10] compatible with current complementary metal oxide semiconductor (CMOS) processes was investigated, and the strain before and after annealing was mainly analyzed with optical[8–12] or x-ray[13] methods.

SOI technology first emerged for radiation hardness for military and space applications, while strained silicon provided carrier mobility enhancement with extreme scaling of MOSFETs. With device scaling and low-power consumption requirements, it is necessary to achieve shallow junctions, low sheet resistance, minimum MOSFET gate/source and gate/drain overlap, and low junction leakage current, requiring high activation of implanted ions. Millisecond annealing is suitable for this since it offers high activation with minimum diffusion for short times at high temperatures.

Since sSOI takes advantage of mechanical bonding during its manufacture, the question arises whether such bonds are resistant to environments typically encountered during wafer fabrication, e.g., high-temperature anneals and other processes that may relieve strain. For this reason we have carried out a series of experiments to test the integrity of such strained SOI layers by using two approaches: high-temperature, short-time thermal anneals and high-dose gamma-ray irradiation. The latter, although not part of Si processing, provides energetic photons that *may* break bonds at the Si/SiO_2 interface, thereby relieving strain.

EXPERIMENTAL PROCEDURES

Samples used in these experiments were made by the layer transfer methods using strained Si on relaxed SiGe donor wafers. The sSi layer had ~0.7%–0.8% biaxial tensile

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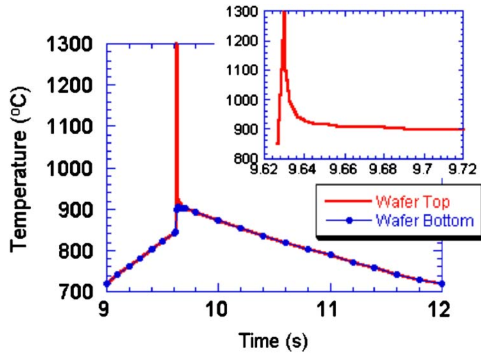


FIG. 1. (Color online) Temperature profile for 1300 °C millisecond anneal.

strain measured by Raman and x-ray diffraction (XRD) from an ~20% Ge fraction in the relaxed SiGe layer. The strained Si film thicknesses were 55 and 80 nm and the buried oxide (BOX) thickness was 145 nm. The sSOI wafers were cut into 1.5×1.5 cm^2 samples for high-temperature annealing and ^{60}Co γ-ray irradiation. The millisecond annealing of the 80 nm samples was done with a flash lamp rapid thermal annealing (RTA) furnace. The samples were ramped at a rate of 150°C/s to 850°C, then the front surface is further heated by ramping to 1200, 1250, and 1300 °C at a rate of approximately 5×10^5 °C/s for millisecond duration anneals.[14] The temperature profile in Fig. 1 for the 1300 °C anneal shows the wafer top and bottom temperatures.

For the 55 nm samples, we used a high-temperature Jipelec rapid thermal annealer with moderate temperature control around 1200–1300 °C. Hence we are not certain of the exact temperatures for these anneals. However, for the "1350 °C" sample in Fig. 2(a), the edges of the sample melted slightly and we estimate the sample temperature to be around 1350 °C or perhaps even slightly higher. Furthermore, the anneal times were in the 1–15 min range, not milliseconds. For gamma-ray irradiation, unstrained SOI and bulk silicon wafers were also irradiated for comparison. The samples were irradiated for a total dose of 51.5 kGy (5.15 Mrad) at a dose rate of 0.23 Gy/s. This dose is higher than usually encountered during semiconductor device radiation experiments. We used it to investigate if such high doses would lead to strain relaxation, as the energetic γ rays ($h\nu \approx 1.25$ MeV) may break Si/SiO_2 bonds of the Si/BOX interface.

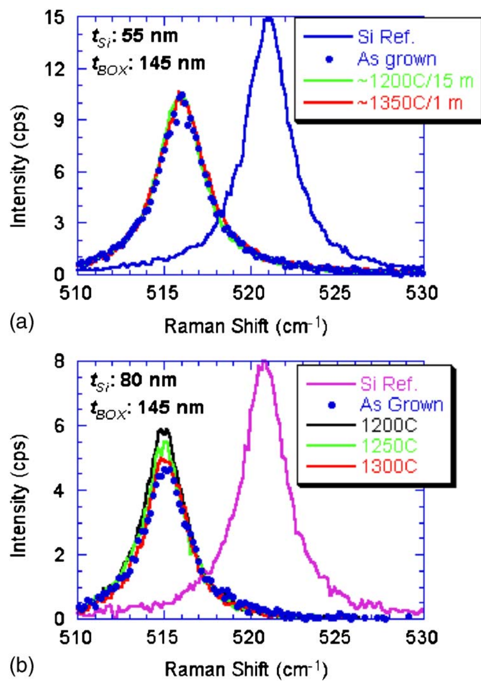
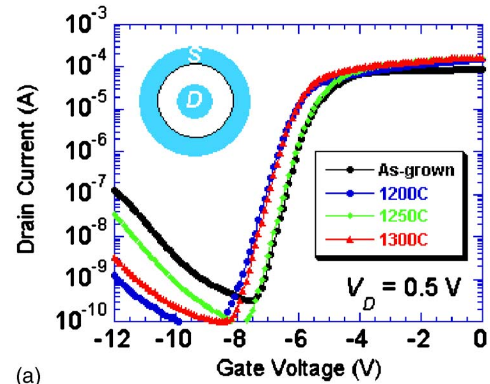


FIG. 2. (Color online) UV Raman spectra for (a) Jipelec RTA and (b) millisecond annealed samples.



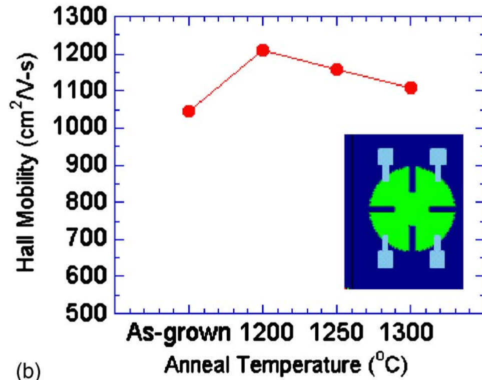


FIG. 3. (Color online) (a) Ring-type Ψ-MOSFET current-voltage characteristics (V_D=0.5 V) and (b) Hall effect mobility. Insets show the device structures.

Ultraviolet (UV) micro-Raman spectra were collected in a direct-backscattering geometry using a 0.8 m triple monochromator equipped with liquid N_2 cooled charge-coupled device detection. A 100× UV objective focuses the 364 nm Ar-ion line and the incident laser power density is reduced to prevent sample heating. The strain and stress are calculated based on the Si LO phonon frequency shift from the bulk Si value of ~520.70 cm^{-1} and a phonon deformation coefficient of −744 cm^{-1} for Si. Along with UV Raman and photoluminescence measurements, electrical parameters, namely, pseudo-MOSFET (Ψ-MOSFET) and Hall mobility were also measured. Ψ-MOSFET measurements are usually made with either point contacts[15] or mercury probes.[16] We have used both of these in the past, but for the experiments reported here, we used evaporated Ti (100 nm)/Al (100 nm) concentric contacts, illustrated in Fig. 3(a). The gate length in this structure, the distance between source and drain, is 20 μm.

Photoluminescence (PL) measurements were carried out with a 364 nm Ar-ion excitation laser. The PL signal from the sample held at 4.2 K was dispersed by a 0.32 m grating

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TABLE I. Measured Raman peak positions and full widths at half maximum (FWHMs) or millisecond annealed samples.

Anneal	Temp. (°C)	Peak pos. (cm^{-1})	Strain (%)	FWHM (cm^{-1})
Jipelec RTA	As grown	515.71	0.67	3.19
	1200	515.64	0.68	3.08
	1350	515.74	0.67	3.22
Millisecond RTA	As grown	515.02	0.76	3.20
	1200	514.90	0.78	2.87
	1250	514.90	0.78	2.92
	1300	515.02	0.76	2.93

monochromator and was detected with an InGaAs photodiode array with resolutions of 0.2 and 2 nm. The basics of the PL technique for SOI wafer characterization were described previously.[17] The samples for the PL measurements were oxidized to 10 nm oxide thickness at 900 °C and then annealed at 450 °C/1 h in forming gas to reduce surface recombination. The PL UV laser-generated electron-hole pairs are confined to the thin Si layer, and radiative PL recombinations competes with radiationless Shockley-Read-Hall (SRH) and Auger recombinations. The aim of PL measurements is to reduce radiationless recombination as much as possible. SRH recombination takes place through defects in the Si layer and at the Si/BOX and Si/oxide interfaces. Forming gas annealing reduces interface states, thereby reducing interface recombination.

EXPERIMENTAL RESULTS

Millisecond anneal

Raman spectra of the Si LO phonons in as-grown and annealed sSOI wafers are shown in Fig. 2. The spectra are fitted with a Lorentzian line shape and linear background functions, with adjustable parameters representing the phonon intensity, width, and frequency. The frequency and widths are summarized in Table I. Based on the frequency and a 20% SiGe donor wafer concentration, the stresses in the as-grown sample are 1.38 GPa for 80 nm and ~1.20 GPa for 55 nm. For the given Jipelec RTA annealing conditions, the sSOI film appears quite stable and the phonon widths are comparable to bulk Si, suggesting excellent sSOI crystallinity, even at the highest temperature. For the millisecond annealing, the stress increases slightly to 1.41 GPa for 1200 and 1250 °C anneals, but remains unchanged from as-grown and 1300 °C. Depending on the anneal temperature and duration, a stress enhancement after anneal is possible[5,7] and is thought to occur because of a reduction in defect density. Also, the phonon widths are narrower by 10% compared to as-grown after the anneal. This is consistent with the idea of reduced defect density as the long-range order increases. Overall, the strain was almost invariable with annealing and the crystal quality was slightly improved. Since the samples came from different parts of a strained 200 mm diameter wafer, it is possible that stress variations across the wafer are reflected in the measurement variations after anneal.

Similar to conventional MOSFETs, the Ψ-MOSFET drain current is determined by carrier mobility, device geometry, oxide thickness, and gate/drain voltages. In addition, the metal source/drain barrier heights influence the I_D-V_G curves. These barriers should be low for electrons for *n*-channel conduction and low for holes for *p*-channel conduction, as also required for Schottky MOSFETs.[18] A given metal contact cannot be both at the same time. Figure 3(a) shows Ψ-MOSFET I_D-V_G characteristics. Electron conduction occurs for $V_G > -8$ V and hole conduction for $V_G < -8$ V. The hole current, being several orders of magnitude below the electron current, is obviously not due to mobility differences but rather is dominated by the Schottky barrier and cannot be used to extract the hole conduction properties, e.g., mobility. The electron drain current exhibits a small increase for the strained and annealed samples but shows no major difference in strain state. The threshold voltage variations, shown by the shift of the I_D-V_G curves, are believed to come from subtle variations of the metal-semiconductor contacts rather than from the Si layer.

The Hall effect provides a direct measurement of electron mobility. Cloverleaf-like van der Pauw patterns were defined on the sSOI photolithographically and etched by reactive ion etch (RIE). Then electron-beam evaporated Ti/Al metal contacts were formed photolithographically. Figure 3(b) shows the measured electron mobility and the device structure. These mobilities are higher than our typical unstrained SOI values. The annealed samples show slightly higher values consistent with Ψ-MOSFET drain currents. The enhanced mobilities of the annealed samples agree well with the UV Raman data. With millisecond annealing, the strain mobilities increase by about 10%.

During PL measurements, each incident photon is assumed to generate one electron-hole pair (ehp). Some of these excess carriers recombine radiatively, emitting photons, while others recombine nonradiatively, emitting phonons. The time constants of these recombination events are the recombination lifetimes, τ_{rad} and τ_{nonrad}. After photons are generated, some may be reabsorbed within the sample. This is typically a very small fraction in Si. Other photons are reflected back into the sample at the surface and others are emitted from the sample to be detected. The external PL efficiency is the internal efficiency times various geometry factors that depend on sample geometry and collection optics. The measured data are, of course, the external efficiencies.

The internal efficiency is given by[19]

$$\eta_{int} = \frac{\tau_{nonrad}}{\tau_{rad} + \tau_{nonrad}}.$$

The radiative lifetime is given by

$$\tau_{rad} = \frac{1}{B(N_A + \Delta n)},$$

where B is the radiative recombination coefficient and Δn the excess minority carrier density. The nonradiative lifetime is given by

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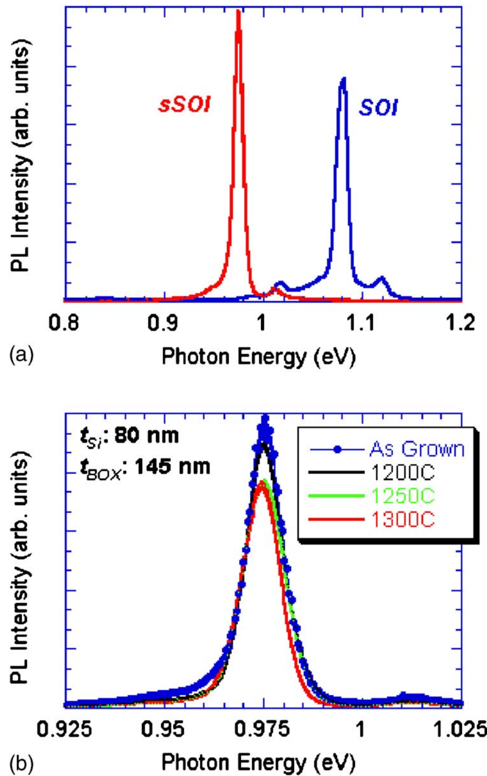

FIG. 4. (Color online) PL spectra with a resolution of 2 nm of (a) SOI and sSOI and (b) sSOI samples under UV light excitation at 4.2 K. sSOI, $t_{\rm Si}=80$ nm and SOI, $t_{\rm Si}=204$ nm.

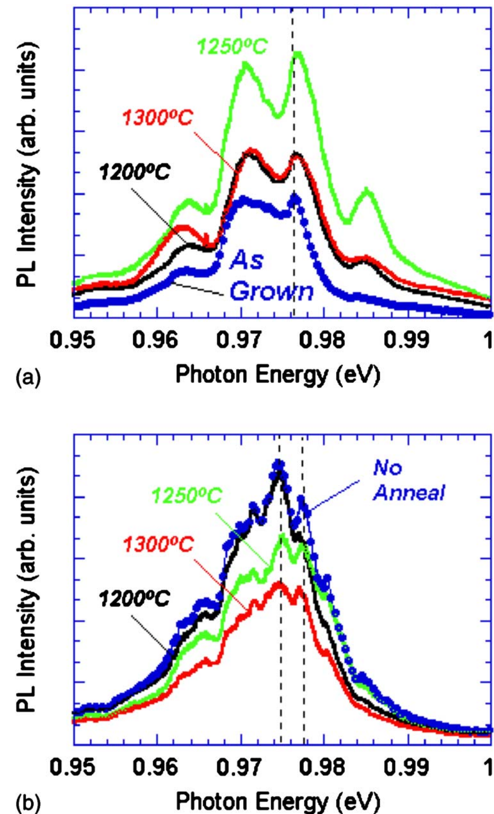

FIG. 5. (Color online) High-resolution PL spectra of the 0.975 eV PL band with a resolution of 0.2 nm. (a) and (b) were obtained from different measurement points under different incident excitation laser angles.

$$\tau_{\rm nonrad} = \left(\frac{1}{\tau_{\rm SRH}} + \frac{1}{\tau_{\rm Auger}} + \frac{1}{\tau_s} \right)^{-1},$$

where $\tau_{\rm SRH}$ is the SRH, $\tau_{\rm Auger}$ the Auger, and τ_s the surface lifetimes. The dependences of the various lifetimes on defect densities are

$$\tau_{\rm SRH} \sim \frac{1}{N_T}, \quad \tau_{\rm Auger} \sim \frac{1}{C_p(N_A + \Delta n)^2}, \quad \tau_s \sim \frac{1}{D_{\rm it}},$$

where N_T is the bulk defect density and $D_{\rm it}$ the interface state density. The question is whether NT and Dit increase during the high-temperature anneal, thus reducing the internal and external PL efficiencies.

Photoluminescence data in Fig. 4(a) show a shift of the band-edge emission wavelength of the strained compared to the unstrained samples. However, there is no substantial difference among high-temperature annealed samples. The 1.08 eV PL band was observed in a conventional SOI wafer (UNIBOND, $t_{\rm SOI}=204$ nm). In contrast, the 0.975 eV PL band appeared for the sSOI wafers. The 1.08 eV PL band in the sSOI wafers could hardly be detected. The 0.975 eV band was observed in all the samples. The shift of the peak wavelength between sSOI and SOI is due to a band gap change with strain.[11] The peak position and half width of the bands were slightly different among the samples, as shown in Fig. 4(b). The peak and half width of the unannealed sample overlapped with those of the 1200 °C annealed sample. The peak positions of the 1250 and 1300 °C annealed samples were slightly higher and lower in photon energy than the peak of the unannealed sample.

As shown in Fig. 5, the PL spectra for a resolution of 0.2 nm varied with measurement points and incident excitation laser angles. Examples of the PL spectra chosen randomly are shown in (a) and (b). We believe that part of the structure in the spectra originates in the interference effect in the thin strained Si layers. The PL spectra of the 1250 °C annealed sample are at a slightly higher energy than the others for both cases. The PL data are in agreement with the other experimental data presented here in that they show no significant shift with the various high-temperature anneals indicative of no measurable band gap shift.

Even though there is some variation in the PL intensities in Fig. 5, the general equivalency of the PL data for the four samples is an indication that no significant bulk or interface defects were generated during the anneals. Increased interface state density may result if some bonds at the Si/BOX interface were dissociated leading to dangling bonds. Also, bulk defects could be introduced during the high-temperature anneals. That does not appear to be the case here.

Gamma-ray irradiation

In addition to high-temperature millisecond annealing, the effect of high-dose γ-ray irradiation on strain relaxation was examined. A γ ray may break Si–O bonds at the sSOI/BOX interface and Si–Si bonds in the sSOI, and therefore may relax the strain in sSOI. The (100) $\rm Si/SiO_2$ interface has $\sim 10^{15}$ bonds/cm^2 and 51.5 kGy γ-ray dose consists of $\sim 10^{16}$ photons/cm^2, which are believed to be sufficient to possibly break some bonds. Four Raman spectra were col-

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TABLE II. Measured Raman peak positions and full widths at half maximum for γ-ray irradiated samples.

Sample	Process	Peak pos. (cm^{-1})	Strain (%)	FWHM (cm^{-1})
Bulk Si	No radiation	520.70	0	3.05
	51.5 kGy	520.66	0.01	3.10
SOI	No radiation	520.71	0	3.28
	51.5 kGy	520.71	0	3.36
sSOI	No radiation	514.88	0.78	3.13
	51.5 kGy	515.02	0.76	3.17

lected from each sample at random locations in order to account, partially, for spatial nonuniformities. The average frequencies and widths are summarized in Table II. Based on the frequency, the strain, stress, and relaxation are calculated. As shown in Table II, the width increase for each sample indicates a slight loss in long-range order due to broken Si–Si bonds and potential displacement of Si atoms from their lattice positions due to nuclear interactions. Figure 6 indicates a blueshift of the phonon frequency due to relaxation of the sSOI layer after irradiation. The relaxation is ~2.5%, which corresponds to ~30 MPa. UV Raman spectra of γ-ray irradiated bulk Si, SOI (not shown here), and sSOI show consistent degradation to the crystalline long-range order after 51.5 kGy exposure with an increase in the phonon widths. We also see fluctuations in the Raman intensity, which can be linked to subtle changes in the refractive index, absorption and transmission coefficients, and the Raman scattering cross section.

Ψ-MOSFET measurements of γ-ray irradiated samples were not made for these heavy dose irradiations. However, measurements for lower irradiation doses on the order of 1 kGy, not shown here, showed significant positive charge creation in the BOX and interface trap generation at the Si/BOX interface. This is likely to be considerably worse for the high-dose irradiations.

CONCLUSIONS

The effects of high-temperature millisecond annealing and high-dose γ-ray irradiation on strain of sSOI wafers were examined by UV Raman, pseudo-MOSFET current-voltage, Hall mobility, and photoluminescence methods.

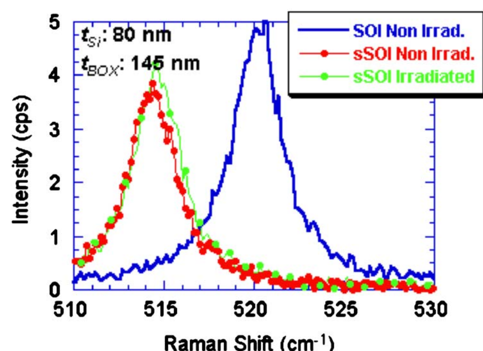

FIG. 6. (Color online) UV Raman spectra for γ-ray irradiated samples.

High-temperature pulse-shape millisecond anneal up to 1300 °C had a little effect on strain in sSOI. UV Raman characterization of millisecond annealed samples showed about 10% reduced phonon widths, indicative of a better crystal quality, which is consistent with electrical measurements. On the other hand, the high-dose 51.5 kGy γ-ray irradiation on sSOI showed subtle relaxation of strain, which is about 2.5% of the fully strained state. However, neither of these "degradation" methods had any significant effect on strain relaxation, suggesting that bonded and strained SOI wafers can easily stand up to conventional Si process temperatures and times.

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