Low-Frequency-Noise Spectroscopy of SIMOX and Bonded SOI Wafers

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***Abstract*—Pseudo-MOSFET structures with metal source, drain, and guard electrodes are used to measure the low-frequency-noise characteristics of Separation by IMplantation of OXygen (SIMOX) and bonded silicon-on-insulator (SOI) wafers. The noise power spectra in the devices made from bonded SOI wafers are almost an order of magnitude lower than those made from SIMOX wafers. This is attributed to the lower interface trap density in the bonded wafers, which is extracted using the unified correlated model. The proposed method can be used to determine the $1/f$ noise characteristics of SOI wafers prior to circuit fabrication.**

***Index Terms*—Buried-oxide (BOX) traps, low-frequency noise (LFN), pseudo-MOSFET, silicon-on-insulator (SOI).**

I. Introduction

SILICON-ON-INSULATOR (SOI) substrates allow faster CMOS circuits to be manufactured in smaller areas with fewer fabrication steps compared to similarly scaled technologies based on bulk substrates [1]. However, the semiconductor industry still favors bulk wafers due to their lower price, easier heat management, and lower defect densities [2]. The defects in SOI wafers at the interface between the silicon channel and the buried-oxide (BOX) layer are particularly important because they may cause excessive low-frequency noise (LFN) in MOSFETs when compared to similar devices on bulk substrate [3]. Usually, the LFN overshoot is only discovered after the manufacturing process is completed.

It would be useful to have a method for measuring the LFN in SOI wafers, which does not require a significant amount of device processing. The pseudo MOSFET is of particular interest in this regard because it allows the dc parameters of the SOI substrate to be measured using a pair of probes placed on the surface of the wafer as the source and drain contacts, whereas the substrate and the BOX form the MOS gate. In one configuration, the drain–current in the pseudo MOSFET flows between sharp-metal probes that behave as point-contact electrodes [4], [5]. Alternatively, liquid-mercury contacts can be used to form low-resistance Schottky contacts to the SOI surface layer [6], [7]. In both cases, it is important to consider the properties of the electrodes and the influence they have on the measurements. For the case of point-contact electrodes, the current is largely controlled by the force applied to the probes, and the current flow path and contact area are not well defined. For the mercury electrodes, the contact area is known, but the current is susceptible to variations in the Schottky-barrier height between the mercury and the silicon. The combination of poor reproducibility and time-varying currents has made it difficult to use pseudo-MOSFET structures for LFN measurements.

We have demonstrated in [8] that by combining metal contacts deposited permanently on the silicon surface with the pseudo-MOSFET approach, it is possible to achieve the long-term current stability and reproducibility required for LFN measurements. Although the permanent contacts to the pseudo MOSFETs require metal deposition and an etch step for device isolation, the processing is quite minimal. In [8], we used permanent-contact pseudo MOSFETs with a ground–signal–ground (GSG) geometry and were able to measure the noise power spectrum of Separation by IMplantation of OXygen (SIMOX) SOI wafers and to extract the interface trap densities. Here, we extend the work by comparing the LFN in bonded and SIMOX SOI wafers biased into accumulation. For currents less than $\sim$10 μA, the noise power spectra are dominated by the hole conduction in the long-channel MOSFET. In this regime, the noise power spectra in the bonded wafer are approximately an order of magnitude lower than that of the SIMOX substrates.

II. Fabrication of the Permanent-Contact Pseudo MOSFETs

In our previous work, the permanent contacts of the pseudo MOSFETs employed a GSG geometry that is commonly used for RF measurements [9]. Here, we have adopted a circular geometry of concentric rings (Fig. 1) which have a number of advantages. For the GSG contacts, some fraction of the current flows at the edges of the etched SOI island that is used to confine the current flow. The LFN measurements therefore include any noise associated with the edges of the device that may not be characteristic of the SOI wafer itself. The edge conduction may also limit the OFF-state current, thereby reducing the current range over which LFN measurements can be made. With the ring geometry of Fig. 1, the current flows from the source electrode to the central drain contact and never sees the edges of the device. The guard ring shown in Fig. 1 is expected

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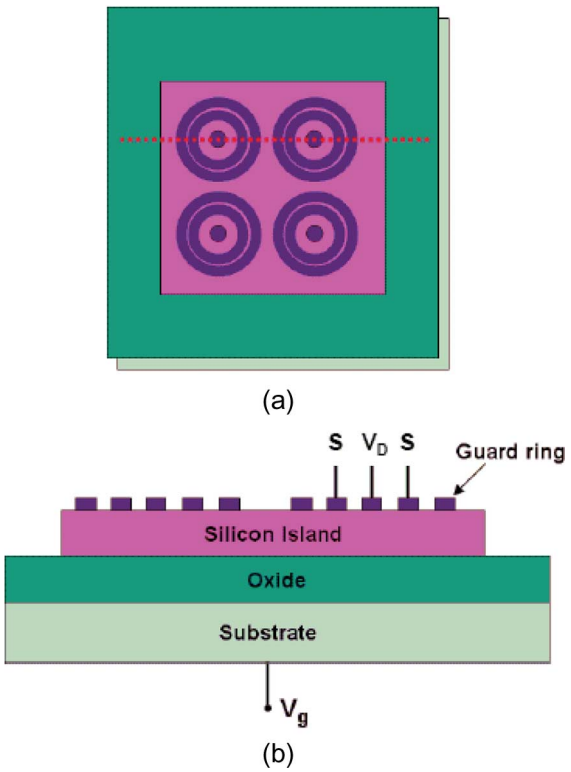

Fig. 1. (a) Top view of the circular MOSFET. (b) Circular MOSFET cross section through the dashed line in (a).

TABLE I
COMPARISON OF THE RESULTS FOR SIMOX AND BONDED SOI WAFERS

Parameter	SIMOX	Bonded SOI
t_{Si}, nm	190	200
t_{BOX}, nm	370	400
N_A, cm^{-3}	5x10^{14}	5x10^{14}
$S_{Vg}(f)$ fitting curve	7.1x10^{-8}/f	1.5x10^{-9}/f
$N_T(E_{Fp})$, cm^{-3}eV^{-1}	2.1x10^{18}	2.6x10^{17}

to reduce stray noise coupling in much the same way that the ground cage of the GSG contact does as discussed in [11].

The fabrication of the permanent contacts is straightforward and begins with p-type bonded and SIMOX SOI wafers, with the specifications given in Table I. Although this paper focuses on p-type substrates, we see no reason why a similar approach could not be applied to n-type SOI wafers. The first step in the processing was to etch down to the BOX layer with reactive-ion etching to create islands in the active silicon layer. The etch consisted of SF_6 at a pressure of 4×10^{-4} mbar for approximately 2.5 min to give a measured etch depth of 200 nm, i.e., the etch terminated at the BOX layer to ensure complete device isolation. Because the current flows between the concentric source and drain contacts, the device isolation etch step could be omitted. Next, an aluminum film 100 nm thick was deposited by electron-beam evaporation and lift-off to create the pattern shown in Fig. 1(a). Finally, a low-temperature anneal in forming gas (450 °C, 30 min) was used to form good Al/Si contacts.

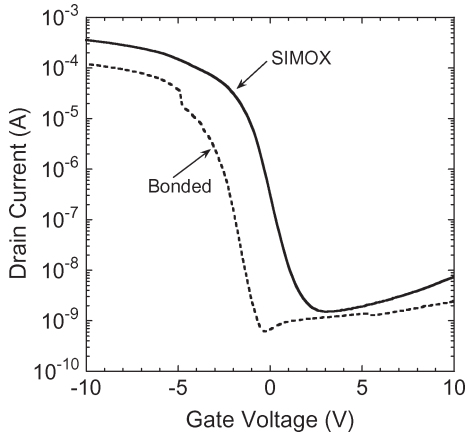

Fig. 2. Circular pseudo-MOSFET drain–current versus gate voltage for devices on SIMOX and bonded SOI wafers at $V_D = -1$ V.

Electrical measurements of the permanent-contact pseudo MOSFETs were performed with a probe station by applying probe needles to the aluminum contacts rather than to the silicon surface itself. Very reproducible I_D–V_G curves were obtained, and Fig. 2 shows an example from a device with a drain contact of radius 50 μm and a source contact with an internal diameter of 120 μm. The SIMOX pseudo MOSFETs are more easily biased into accumulation than those on the bonded substrate and therefore have higher drain–currents at a given substrate voltage. This is in part due to the thinner BOX layer (370 nm for SIMOX and 400 nm for the bonded SOI wafers), although differences in the background doping concentration and oxide charges will contribute as well. The I_D–V_G curve of the bonded device showed a clearly visible kink at a gate voltage of approximately -5 V (Fig. 2). Kinks such as this are often observed in pseudo MOSFETs [10] and are caused by the change in the BOX capacitance when the depleted region on the substrate side of SOI vanishes over a small range of the gate voltage. This effect is more pronounced for bonded pseudo MOSFETs due to the sharper BOX/substrate interface.

In Fig. 3, we show the transconductance g_m as a function of drain–current for both the bonded and SOI pseudo MOSFETs. At lower drain–currents, the transconductance of the bonded pseudo MOSFETs is higher than that of the SIMOX devices. At currents higher than 100 nA, the transconductance of the SIMOX pseudo MOSFETs exceeds that of the bonded device up to the point of the kink, above which the g_m values of both devices are similar. The measured g_m shown in Fig. 3 is used to extract the gate-referred noise power spectrum as described below.

III. MEASUREMENT OF THE DRAIN–CURRENT NOISE SPECTRAL DENSITY

The low-frequency drain–current noise spectral densities (S_{Id}) of the permanent-contact pseudo MOSFETs were measured using the method developed by Blaum *et al.* [11] and described in detail in [8]. For the SIMOX devices, S_{Id} follows an approximately $1/f$ behavior for currents in the range of 0.1–20 μA. At high currents, the slopes are steeper than $1/f$

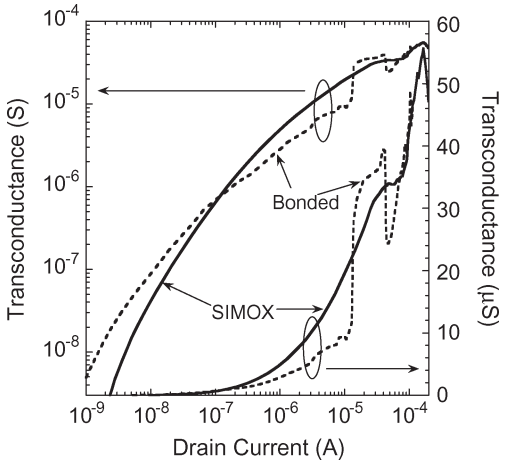

Fig. 3. Circular pseudo-MOSFET transconductance as a function of drain–current for devices on SIMOX and bonded SOI wafers at $V_D = -1$ V.

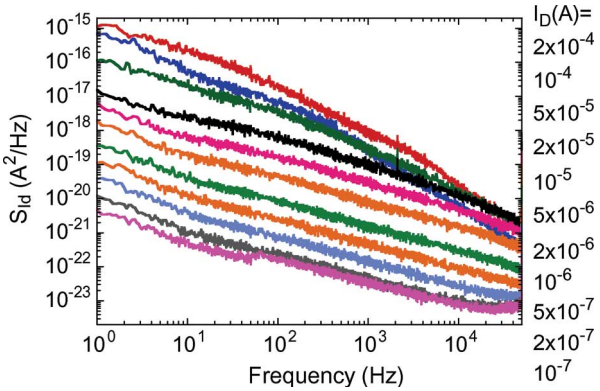

Fig. 4. $S_{\rm Id}$ versus frequency at $V_D = -1$ V for the SIMOX circular pseudo MOSFET.

(Fig. 4). Similarly, the pseudo MOSFETs on the bonded wafer have $1/f$ behavior at lower currents with steeper slopes when biased above 10 μA (Fig. 5). Usually, a $1/f$ slope suggests a uniform trap distribution in the BOX layer at a given energy level [12]. Steeper slopes can be explained by a nonuniform distribution of traps in the BOX layer at higher energies [13].

The noise power spectral density at a frequency of 1 Hz is shown in Fig. 6 for both devices as a function of drain–current. The devices show similar trends, with $S_{\rm Id}$ being proportional to I_D^2 for currents above $\sim$5 μA corresponding to accumulation of the active Si/BOX interface (Fig. 3). This $S_{\rm Id} \propto I_D^2$ is consistent with the LFN behavior of bulk MOSFETs [12], [13]. However, the slopes of $S_{\rm Id}$ are proportional to $I_D^{1.5}$ for $I_D < 5$ μA for which both devices are expected to be biased into the volume conduction regime. These lower slopes can be explained by the reduced influence of the BOX traps on the active carriers at lower absolute gate voltages. Notably, the values of $S_{\rm Id}$ for the bonded circular pseudo MOSFET are approximately an order of magnitude lower than for the SIMOX device (Fig. 6), which suggests lower trap densities in the BOX of the bonded SOI wafer compared with the SIMOX wafer. The trap densities are extracted from the gate-referred noise power spectrum as described in Section IV.

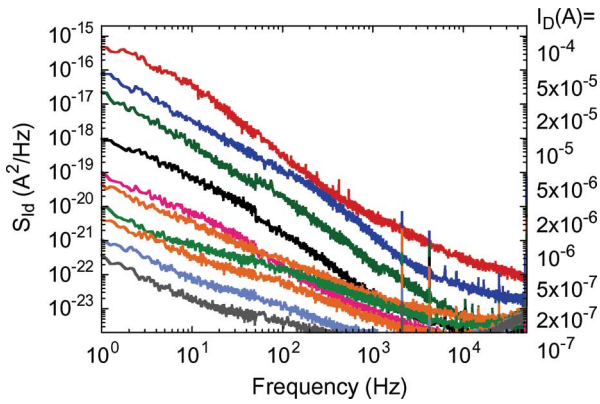

Fig. 5. $S_{\rm Id}$ versus frequency at $V_D = -1$ V for the bonded circular pseudo MOSFET.

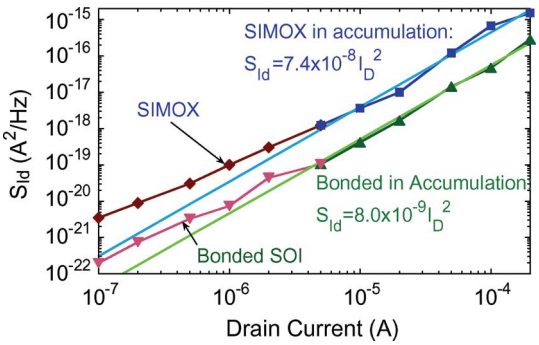

Fig. 6. $S_{\rm Id}$ versus I_D at $f = 1$ Hz for the SIMOX and bonded circular pseudo MOSFETs.

IV. Gate-Referred Voltage-Noise Spectral-Density Calculations and Analysis

The gate-referred voltage-noise power spectrum $S_{\rm Vg}$ is determined from $S_{\rm Id}$ and the circular pseudo-MOSFET transconductance g_m [13] (Fig. 3) using the relation $S_{\rm Vg} = S_{\rm Id}/g_m^2$. For the case of the SIMOX pseudo MOSFET, the $S_{\rm Vg}$ curves are closely grouped together (Fig. 7) which is similar to the behavior of $S_{\rm Vg}$ in long-channel MOSFETs with bulk silicon substrates [12], [13]. For the bonded pseudo MOSFET, the $S_{\rm Vg}$ versus frequency data are clustered into two groups: one for currents below 10 μA that follow a $1/f$ behavior, and another cluster for higher currents with a steeper slope. As with the $S_{\rm Id}$ data for the bonded pseudo MOSFETs (Fig. 5), the cluster of data in Fig. 8 with the steeper than $1/f$ slope is believed to be due to a nonuniform distribution of traps in the BOX layer at higher energies and/or possibly the Schottky contacts dominating the LFN $S_{\rm Vg}$ spectra.

When biased into accumulation, the $S_{\rm Vg} \propto 1/{\rm f}$ LFN behavior can be explained by the unified correlated model [14] where the carrier number and mobility fluctuations are taken into account in a correlated fashion

$$S_{\rm Vg}(f) = \frac{kTq^2}{\gamma f {\rm WL} C_{\rm BOX}^2}(1 + \alpha\mu_{\rm eff}N)^2 N_T(E_F). \quad (1)$$

In (1), γ is the attenuation coefficient, $\mu_{\rm eff}$ is the effective carrier mobility, α is the coulombic scattering parameter, N is the

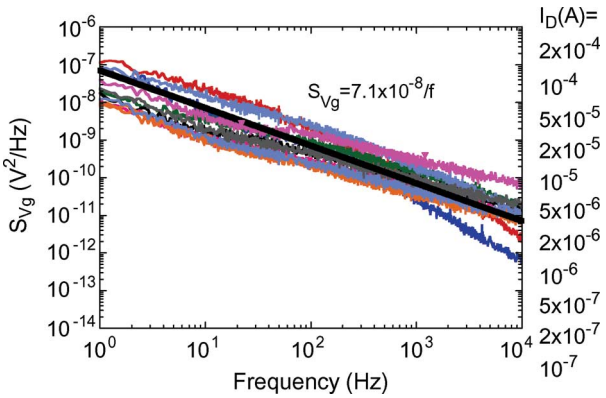

Fig. 7. S_{Vg} versus frequency at $V_D = -1$ V for the SIMOX circular pseudo MOSFET. The thick black line and the formula show the approximation of curves in accumulation.

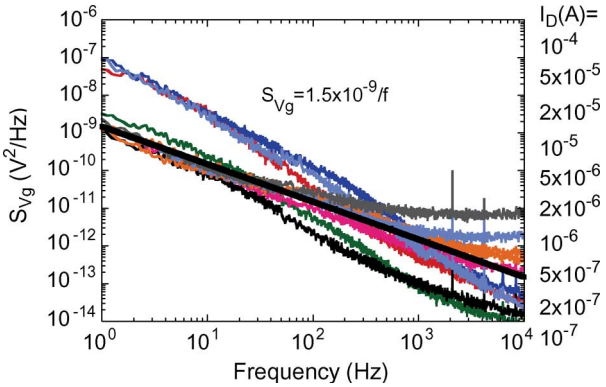

Fig. 8. S_{Vg} versus frequency at $V_D = -1$ V for the bonded circular pseudo MOSFET. The thick black line and the formula show the approximation of curves in accumulation.

number of channel carriers per unit area, C_{BOX} is the BOX capacitance per unit area, WL is the gate area, and $N_T(E_F)$ is the oxide-trap density (per cubic centimeter per electron volt) [14]. The data in Figs. 7 and 8 have been fitted to an equation of the form $S_{\mathrm{Vg}} = C/f$, where C is the amplitude of the flicker noise at 1 Hz. The fit was applied to the S_{Vg} data measured at $I_D = 10\ \mu$A. This particular bias current was chosen because it is high enough to ensure that the device is in accumulation but lower than the value at which the LFN shows steeper than $1/f$ behavior. The resulting fits are shown as solid lines in Figs. 7 and 8 and broadly reflect the behavior of S_{Vg} for both the SIMOX and bonded wafers over a wide range of currents.

The BOX capacitance $C_{\mathrm{BOX}} = \varepsilon_{\mathrm{SiO2}}\varepsilon_o/T_{\mathrm{BOX}}$ and the channel carrier density $N = C_{\mathrm{BOX}}(V_{\mathrm{gs}} - V_{\mathrm{th}})/q$ are found from the dimensions and biasing conditions of the permanent-contact pseudo MOSFETs. The calculation procedures and physical meaning of the attenuation coefficient γ and the coulombic scattering parameter α are described in [15]. Published data are used for the effective carrier mobility μ_{eff} [16]. Depending on the device and the biasing conditions, the $\alpha\mu_{\mathrm{eff}}N$ product varies from ∼0.09 to ∼0.21. Thus, in all cases, we have to account not only for the random fluctuation of carrier density but also for the correlated mobility fluctuation. The interface and border trap density at the quasi-Fermi level $N_T(E_{\mathrm{Fp}})$ is extracted as $N_T(E_{\mathrm{Fp}}) = 2.1 \times 10^{18}\ \mathrm{cm}^{-3} \cdot \mathrm{eV}^{-1}$ for the SIMOX devices and $2.6 \times 10^{17}\ \mathrm{cm}^{-3} \cdot \mathrm{eV}^{-1}$ for the bonded circular pseudo MOSFETs. The $N_T(E_{\mathrm{Fp}})$ values are higher than for a usual MOSFET gate oxide, which are typically $1 \times 10^{17}\ \mathrm{cm}^{-3} \cdot \mathrm{eV}^{-1}$ [17].

V. Conclusion

LFN is measured on SIMOX and bonded SOI wafers by the pseudo-MOSFET method using evaporated metal contacts. This device yields very useful results with minimal fabrication. Trap densities have been extracted for the bonded and SIMOX wafers with SOI layers of ∼200 nm thick, typical of those used for partially depleted (PD) SOI CMOS technologies. We find higher noise on SIMOX wafers due to higher BOX bulk and interface trap densities. The higher trap densities may be due to the fact that the SIMOX wafers are from an older technology than the bonded wafers and may not reflect the quality of newer SIMOX wafers. The results of LFN spectroscopy of the SIMOX and bonded SOI wafers are summarized in Table I. The proposed method can be used to study the influence of radiation and a variety of treatments on PD SOI wafers and for research of Schottky-barrier MOSFETs [18]. For substrates in which the silicon channel is thinner than the depletion region, as in fully depleted SOI CMOS, the influence of traps in the native oxide on the surface of the wafer [15] will need to be taken into account.

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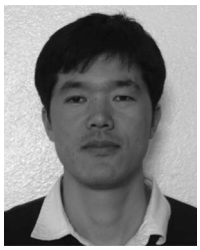

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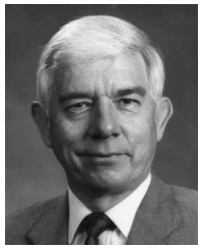

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