Pseudo-MOSFET Substrate Effects of Drain Current Hysteresis and Transient Behavior

Kihoon Park, Pinakpani Nayak, Sorin Cristoloveanu, *Fellow, IEEE*, and Dieter K. Schroder, *Life Fellow, IEEE*

***Abstract*—A large drain current-gate voltage hysteresis of evaporated metal contact pseudo-MOSFETs (Ψ-MOSFET) is reported. The Ψ-MOSFET drain current exhibits a hysteresis when the gate voltage is swept from negative to positive and from positive to negative voltages. Optical illumination, elevated temperatures, and decreased sweep rate during the measurements eliminate this phenomenon. The reason for this behavior is related to electron–hole pair generation in the substrate. In this paper, we report systematic studies and device simulations to document and understand these substrate effects during Ψ-MOSFET measurements.**

***Index Terms*—Carrier generation, drain current, hysteresis, MOSFET, pseudo-MOSFET.**

I. Introduction

DRAIN CURRENT transients are frequently observed in SOI MOSFETs. Most commonly, these transients are attributed to the floating Si body coupled with impact ionized carriers at the reverse-biased body–drain junction. Such floating-body transients have been proposed for capacitorless DRAMs originally promoted by Okhonin *et al.* [1]. A recent review is given by Bawedin *et al.* [2]. An important aspect of such devices is the retention time, which is related to the floating-body generation lifetime. This time should be as long as possible to minimize DRAM refresh cycles, e.g., 10–100 s at room temperature

The Ψ-MOSFET is a simple, yet effective, test structure to determine a variety of Si film and film/oxide properties. In its simplest form, it consists of two probes placed on the Si film forming the source and drain, the substrate being the gate and the buried oxide (BOX) functions as the gate oxide [3]. Other implementations use Hg probes [4], evaporated metal films for source/drain contacts [5], or four probes [6]. In all cases, the source and drain are Schottky diodes, not ohmic contacts (except for pressure-adjustable probes), as the Si film is usually lightly to moderately doped.

Since the substrate is the gate, one may expect surface conditions of the substrate at the BOX/substrate interface to play a role in the device operation, particularly during the transients. For example, for p-type substrates with negative gate bias, the substrate is driven into depletion, inversion, or deep depletion, depending on whether the gate voltage is in steady state or suddenly applied. As transient Ψ-MOSFET measurements are used to determine the generation and recombination parameters of the Si film [7]–[9], it is important to understand what role the transient substrate properties play during such measurements.

Barth and Angell were among the first to use deep-depletion measurements to characterize SOI-like devices [10]. Ioannou *et al.* drove the SOI MOSFET with top and bottom gates from depletion or accumulation to stronger accumulation to create a deep-depletion condition to extract the generation lifetime and surface generation velocity. They mention that a deep-depletion layer can also be created in the substrate following the bias step and suggest the elimination of this by applying the bias step on the front gate instead of the back gate [11]. Munteanu and Ionescu show that both generation and recombination lifetimes can be extracted from appropriately biased transients [12]. Most of the published papers use partially depleted SOI films. Yasuda *et al.* show that the generation lifetime in fully depleted films can also be characterized [13]. Sato *et al.* step the gate voltage from positive voltage to zero. The resulting drain–current decay is attributed to the recombination in the SOI film [14]. To our knowledge, the role of the substrate during transient measurements has not been discussed before. It is not clear to us why others have not seen or, at least, not reported it.

We have observed a hysteresis in the drain current-gate voltage characteristics, where gate voltage refers to the voltage applied to the substrate. As shown in Fig. 1, when the gate voltage is swept from positive to negative voltage, the drain current temporarily lies above the negative to positive swept current. This is a transient phenomenon with the hysteresis loop becoming narrower as the sweep rate is reduced, and it disappears when light is shone on the device. This phenomenon puzzled us when we first observed it, and we propose an explanation in this paper. After examining various possible causes (transient effects in Si film, BOX, and substrate), we believe it to be associated with substrate depletion/inversion. Selected experiments reported as follows confirm this scenario.

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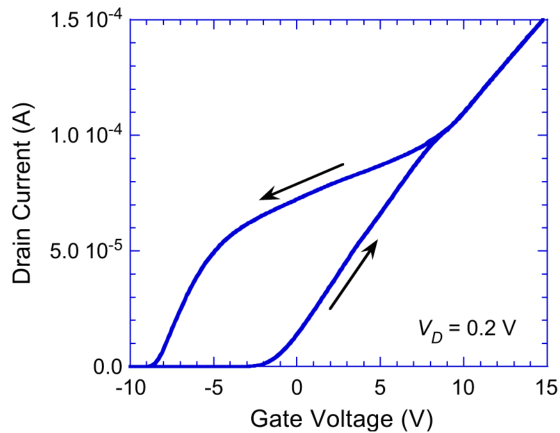


Fig. 1. Typical I_D–V_G curves for Ψ-MOSFETs with no top gate. The arrows indicate the gate voltage sweep directions.

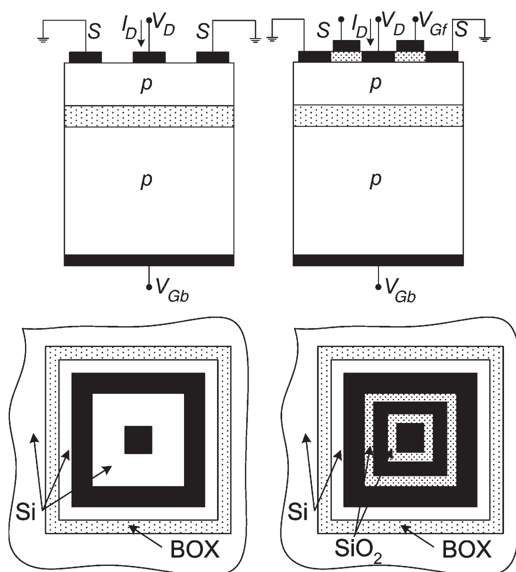
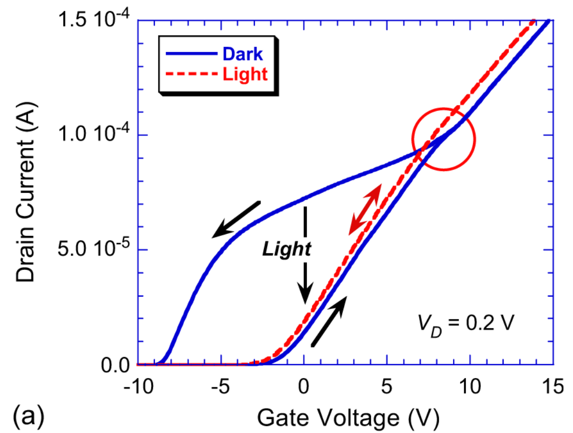


Fig. 2. Cross-sectional and top views of (left) "no top gate" and (right) "top gate" devices. Sample dimensions: (Left) Drain is the centered 100 μm × 100 μm square, and the next rim is the source with 100-μm width. The gap between drain and source is 100 μm; (right) the central rim is the top gate with 10-μm gaps between drain and source gates.



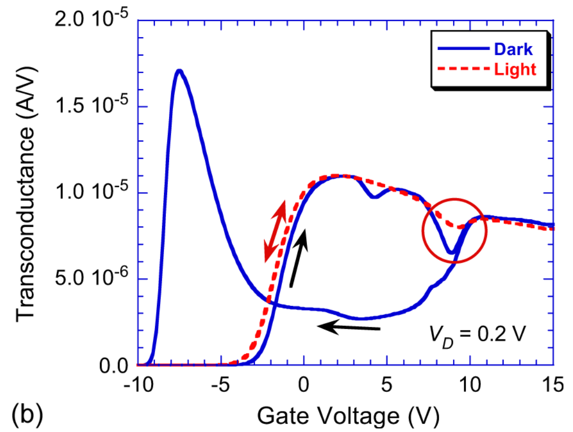


Fig. 3. Typical (a) I_D–V_G and (b) g_m curves for "no top gate" devices. The arrows indicate the gate voltage sweep directions.

II. Experimental Procedures

We used two types of SOI samples, which are strained SOI (sSOI) and unstrained SOI. The sSOI is a bonded SOI and has Si film and BOX thicknesses of $t_{\mathrm{Si}} \approx 80$ nm and $t_{\mathrm{BOX}} = 145$ nm, respectively, and $N_A \approx 10^{15}$ cm^{-3} for both Si film and substrate. The Si film is strained to ~1.4 GPa stress without SiGe layer. The normal unstrained SOI has about the same sample specification with sSOI, except for the strain. We made two types of device structures: devices with and without top gate, shown in Fig. 2. Most of the discussion in this paper deals with the "no top gate" structure.

The sSOI and SOI samples were dry oxidized at 900 °C for oxide thicknesses of 50 and 30 nm to form top gate oxides for top-gated devices. After oxidation, the thicknesses were measured as SiO_2/Si/BOX = 54/53/145 nm for sSOI and 29/76/145 nm for unstrained SOI. Then, the device area was isolated from the rest of the samples to reduce possible leakage current through BOX pin holes or sample edge by etching the top thermal oxide and Si film with buffered oxide etchant (BOE) and reactive ion etching. In the case of the "no top gate" structure, the thermal oxide was etched with BOE. The outermost dotted rims in the images in Fig. 2 are the exposed BOX layers. The metal contacts are then defined by photolithography. Finally, 150-nm Ti/ 100-nm Al metal contacts were e-beam evaporated on the bare Si surface (and top gate oxide in the case of top gate structure). The innermost 100 μm × 100 μm square serves as the drain, and the outermost contact serves as the source. For the top gate structure, the middle rim deposited on the thermal oxide serves as a second gate to control the top interface properties. After metal deposition, samples were forming gas ($5\%\ H_2 + 95\%\ N_2$) annealed at 400 °C/20 min. All electrical measurements were made in a dark Micromanipulator probe station at room temperature with an Agilent 4155C parameter analyzer. The integration time for the measurement unit was set to default long, and the hold time was typically 100 s for these measurements, unless stated otherwise in this paper.

III. Results and Discussions

Typical drain current-gate voltage (I_D–V_G) characteristics for "no top gate" devices are shown in Fig. 3. Both sSOI and SOI have qualitatively the same hysteresis characteristics. When the gate voltage is swept from negative to positive (forward) value, we find a small kink in the "dark" curve, shown in

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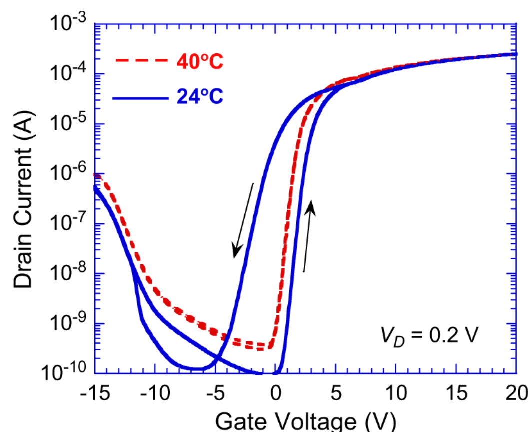

Fig. 4. Temperature-dependent I_D–V_G characteristics of "no top gate" devices. The arrows indicate the gate voltage sweep directions.

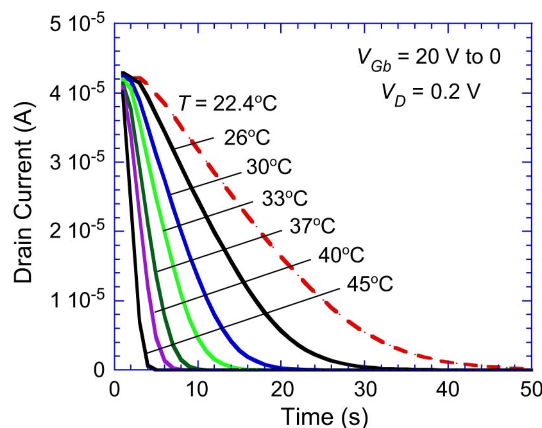

Fig. 5. Normalized drain current transient as a function of temperature.

the circle. Sweeping from positive to negative (backward), for example, from 15 to -10 V, the "dark" curves in the backward sweep directions coincide, until the gate voltage reaches the kink, beyond which the hysteresis forms. The curves measured with light on the device exhibit no hysteresis. The arrow indicated as "Light" in Fig. 3(a) shows that, if the light is turned on at, for example, 0 V, the current drops immediately and the hysteresis disappears. Fig. 3(b) shows the transconductance (g_m) of the curves in Fig. 3(a), and we see a dip at the same gate voltage ($\sim$9 V) as the kink. The "light" curve also shows a small dip, but this is much attenuated compared to the dark curve. "Light" refers to measurements made with the probe station microscope light on during the measurement. A dip in transconductance is known to happen when the BOX–substrate interface enters depletion [3]. The coincidence of the hysteresis onset and transconductance dip points out that the main effect occurs within the substrate.

A different type of hysteresis, which is the metastable dip, has been observed by Bawedin *et al.* [15]. It is found in fully depleted SOI MOSFETs with top and bottom gates, when the top interface moves from accumulation to inversion with the bottom interface biased into inversion. It manifests itself as a transconductance dip and does not occur when the top interface moves from inversion to depletion. In that sense, it is opposite to our observed hysteresis. It also requires two gates, whereas we observe our hysteresis with only a bottom gate and a free top surface. It is, of course, well known that the threshold voltage of fully depleted SOI MOSFETs depends on the condition of the bottom Si film/BOX interface, i.e., whether that interface is inverted, depleted, or accumulated [16]. The effect of the substrate on capacitance and threshold voltage has also been discussed [17], [18], but its effect on transient behavior has not.

Next, we measured the I_D–V_G curves at various temperatures, shown in Fig. 4, for a different device on the same wafer. The hysteresis is reduced for the higher temperatures similar to the behavior with illumination. This hysteresis reduction or elimination suggests an electron–hole pair (ehp) generation mechanism which is enhanced by optical and thermal generation. Then, we changed the gate voltage from $+20$ V to 0 in one step and monitored drain–current transient as in Fig. 5. These transients are clearly temperature dependent, with the recovery time reduced at higher temperatures. With increasing temperature, we propose the transient reduces due to enhanced ehp generation in the substrate. The ehps are generated in the substrate space-charge region and possibly at the BOX/substrate interface. With light, the transient decay time approaches zero. Note that we see little hysteresis in the hole conduction region (-15 to -10 V or so).

If substrate generation dominates the hysteresis, then changing the substrate generation rate should influence the I_D–V_G data. Light and temperature increase the generation rate, and decreasing the sweep rate provides more time for ehp generation in the substrate. All of these should diminish or eliminate substrate deep depletion. As shown in Fig. 6(a), backward sweeps approach forward sweeps as delay times increase, because the substrate has more time to reach steady state. Here, we did not repeat forward sweeps with different delay times, as they do not change with the sweep rates. The delay time is the time required for the device under test to settle after stepping the input. The change of the substrate deep depletion to inversion states leads to a generation current which is detected as a gate current. The back-gate currents, corresponding to the drain current in Fig. 6(a) and shown in Fig. 6(b), decrease with increasing sweep delay time as one would expect, since the generation current is low for low sweep rates approaching zero as equilibrium is approached.

Complementary to the current measurement, we also measured the C–V and C–t data of a MOS capacitor (MOS-C) located next to the Ψ-MOSFET. For this device, we etched the entire Si film and deposited an Al gate directly on the BOX, forming a conventional MOS-C. For the C–t curve, the MOS-C is pulsed into deep depletion, and the capacitance–time curve is measured, as shown in Fig. 7. A thorough review of this technique can be found in [19]. The existence of a capacitance transient confirms once more that the substrate is in deep depletion for this bias condition. We did not extract the generation lifetime but merely use the C–t curve to see the length of the transient, which, in this case, is due to ehp generation in the substrate following a 10 V gate step. The room-temperature transient times are about 50 and 55 s for both the Ψ-MOSFET drain current and MOS-C capacitance, suggesting that *substrate* ehp generation is responsible for the drain current hysteresis and transient.

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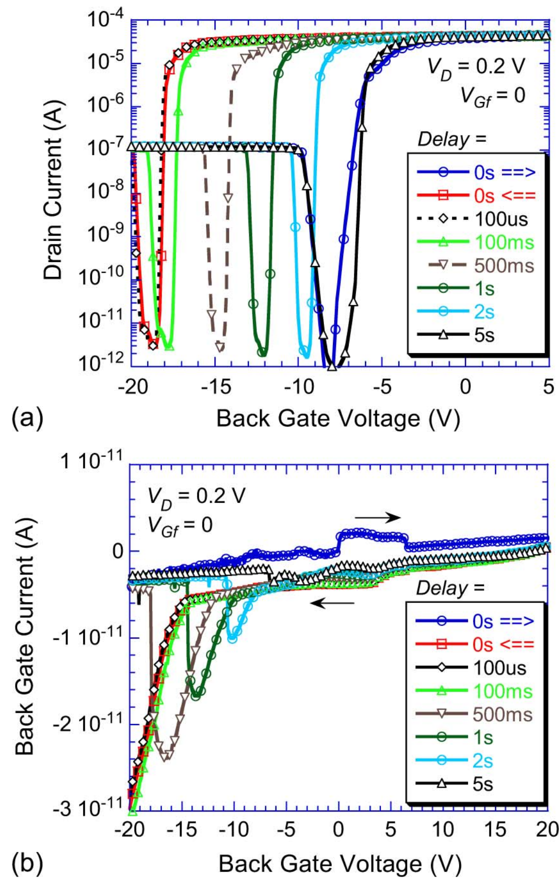

Fig. 6. (a) Drain and (b) back-gate currents as a function of delay time for a device with top gate. In (a), the positive gate voltage is only shown to 5 V for clarity; the device was actually biased to 20 V. The device is initially held at the starting voltage, e.g., −20 V, for 100 s.

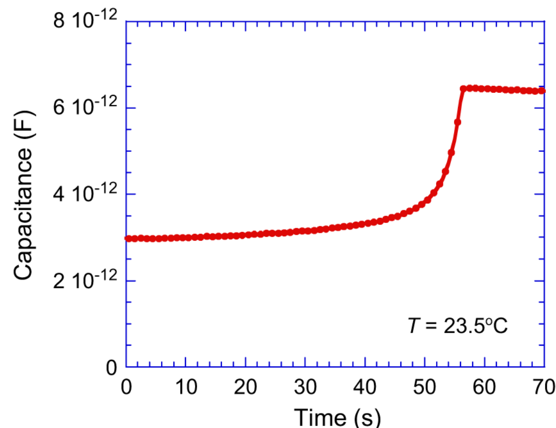

Fig. 7. Time dependent capacitance characteristic of a MOS-C next to the Ψ-MOSFET. The MOS-C gate voltage was held at −10 V for 10 s and then switched to 10 V.

Fig. 8 shows the I_D–V_G curves of an unstrained device with top gate and $V_{\rm Gf} = 0$. It also shows the hysteresis in relation to the "kink." In this case, the back-gate voltage was swept from −5 to +20 V and then swept back to −5 V. A 100 s holding time was applied at the start of both forward and backward sweeps, ensuring steady state as the substrate transient has dissipated within this time. As shown here, we have to be above the "kink" not to see a hysteresis. In Fig. 8(b), the device was swept from

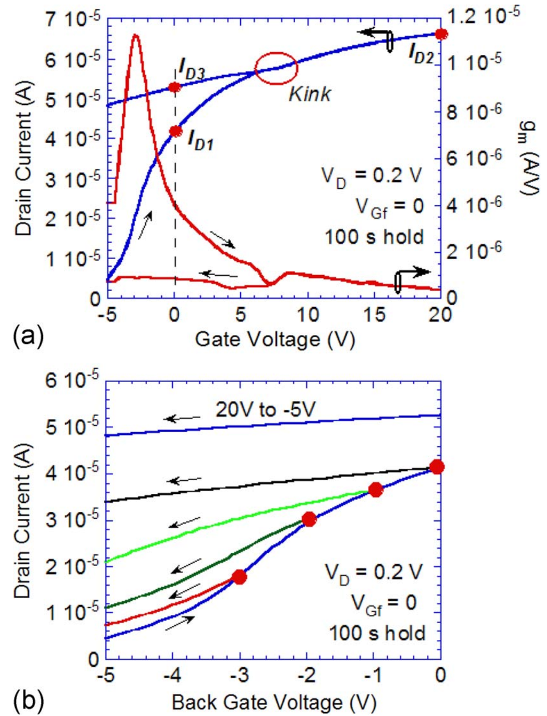

Fig. 8. (a) Typical I_D–V_G and g_m. (b) Drain current hysteresis characteristics as a function of backward sweep starting voltages of top-gated devices.

−5 V to 0 and then back to -5 V and also −5 V to −1, −2, −3, and then back to −5 V. Again, before each sweep, the device was held at the starting voltage for 100 s. The current from the +20 to −5 V backward sweep is also shown for comparison. These graphs show that, if one starts a backward scan below the kink point, the drain current hysteresis is always observed. With incident light, all of these hysteresis effects disappear. It is also obvious from these results that the forward sweep exhibits no hysteresis, obeying steady state.

IV. Proposed Mechanism for the Drain–Current Hysteresis

After a thorough investigation of the results, we propose a possible mechanism for the Ψ-MOSFET drain current hysteresis behavior. Fig. 9(a) shows the device cross section for $V_{\rm Gb} = 0$, where $V_{\rm Gb}$ is the back-gate voltage. We distinguish between back and front gates, because some of our devices have both gates, although this one does not. Positive BOX charge, indicated by $Q_{\rm ox}$, inverts both the Si film and the substrate. In this simple example, 12 oxide charges induce 12 inversion charges, six in the film and six in the substrate; we neglect the charge in the space-charge regions here for simplicity. The drain current, shown in Fig. 8(a), is I_{D1} for this case. The negative threshold voltage in Fig. 8(a) is due to the positive BOX charge.

When $V_{\rm Gb}$ is changed from zero to +20 V, the substrate is driven into accumulation, and since the sum of the charges is zero, the Si film inversion charge increases, as shown in Fig. 9(b), and the drain current increases to $I_{D2} > I_{D1}$, Fig. 8(a). When the gate voltage returns to $V_{\rm Gb} = 0$, $Q_{\rm ox}$ wants to induce the same channel in the Si film and substrate, as

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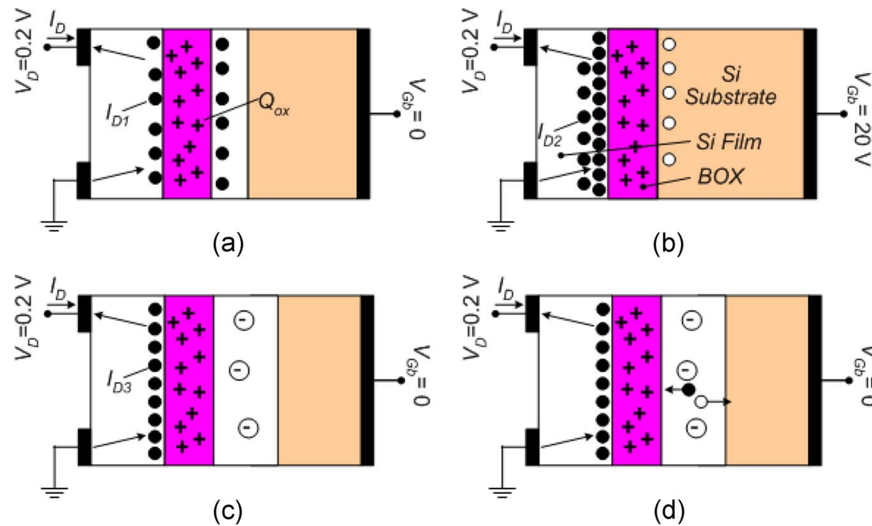

Fig. 9. Device cross sections indicating the various charges in the Si film, BOX, and substrate. The white regions in the Si film and substrate indicate space-charge regions. (a) $V_{\rm Gb} = 0$; $I_D = I_{D1}$. (b) $V_{\rm Gb} = 20$ V; $I_D = I_{D2}$. (c) $V_{\rm Gb} = 0$; $I_D = I_{D3}$. (d) $V_{\rm Gb} = 0$; I_D approaches I_{D1} as t tends to ∞.

in Fig. 9(a). However, there are few electrons in the substrate to form an inversion layer, and the substrate goes into deep depletion, as shown in Fig. 9(c), with a substantial voltage drop across the deep-depleted space-charge region. Since the charge in the substrate space-charge region in Fig. 9(c) is less than that in the substrate inversion channel in Fig. 9(a), more inversion charge must exist in the Si film for charge balance. Hence, the drain current is now I_{D3}, which is lower then I_{D2} but higher than I_{D1}. The deep-depleted substrate space-charge region gradually collapses due to ehp generation, shown in Fig. 9(d). The substrate inverts, leading to an approximate $2\phi_F$ final voltage drop; the voltage drop across the Si film increases, and the drain current gradually returns to I_{D1}. Hence, the drain current transient is governed by substrate ehp generation. The transients in Figs. 5(a) and 7 have about the same recovery time, supporting this idea, even though these transients were measured on different devices with different techniques. However, both are determined by substrate ehp generation. Our top gate structure behavior is different; it is similar to Bawedin *et al.* [15], when the top gate voltage is swept instead of the back gate. However, when the back-gate voltage is swept for this device, it behaves like a "no top gate" device, since the top gate plays no role during this measurement. With top gate voltage sweep, there is no back-gate (substrate) depletion, and the device behavior is only governed by interface coupling of the Si film.

The drain current transient can also be monitored by the back-gate current, as shown in Fig. 6(b). As shown in Fig. 9(d), with the substrate in deep depletion, this is a nonequilibrium state, and ehp generation leads to substrate or gate current. With increasing delay time (decreasing sweep rate), the substrate is driven less into deep depletion, the gate current reduces, and its peak disappears. Note that the hysteresis onset or transconductance dip reflects the transition from accumulation to depletion at the BOX–substrate interface and can be used for extracting the flatband voltage, doping density, and oxide charge.

A final confirmation is obtained with light measurements. We know that visible light, which penetrates deeply into the substrate, diminishes or extinguishes the hysteresis (Fig. 3) and reduces the transient time. By contrast, ultraviolet light, if entirely absorbed in the Si film, should have no effect as it does not penetrate into the substrate. We shone 254-nm UV light on the device. Its absorption coefficient is $\alpha \approx 2 \times 10^6$ cm^{-1}, giving an absorption depth of ~5 nm. This light should be largely absorbed in the Si film and hence should have little effect on substrate ehp generation and hysteresis. We do, however, see an effect, as shown Fig. 10. The light reduces the hysteresis. How can that be?

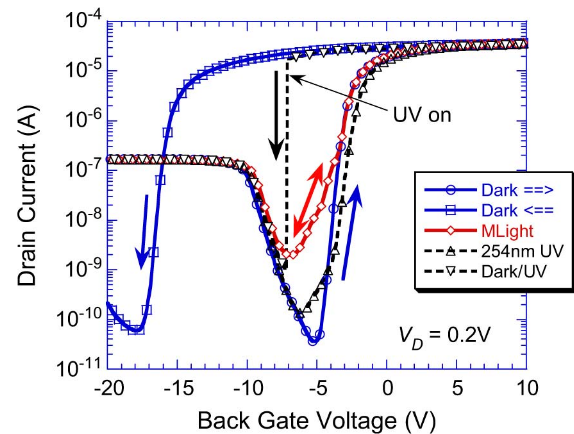

Fig. 10. I_D–V_G characteristics depend on light sources. The "Dark/UV" refers to the measurement made in the dark from 10 to −7 V, and then, the UV light is turned on.

The UV light intensity in the substrate is $\Phi = (1 - R)\Phi_0 \exp(-\alpha t_{\rm Si})$, where Φ_0 is the incident photon flux density. We assume no absorption in the BOX. For $t_{\rm Si} = 70$ nm, we find $\Phi/\Phi_0 \approx 5 \times 10^{-7}$. The optical power of ~ 100 μW corresponds to $\Phi_0 \approx 10^{13}$ photons/s $\cdot$ cm^2, giving ~ 5×10^6 photons/s $\cdot$ cm^2 for the photons penetrating into the substrate after absorption in the Si film. The thermal generation rate is $G_{\rm th} = n_i W/\tau_g$ ehp/s $\cdot$ cm^2. For $n_i = 10^{10}$ cm^{-3}, $W = 2$ μm, and $\tau_g = 10$ μs, $G_{\rm th} = 2 \times 10^{11}$ ehp/s $\cdot$ cm^2, which is significantly higher than the optical generation rate of

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5×10^6 ehp/s $\cdot$ cm^2, assuming each UV photon absorbed in the substrate creates one ehp. However, as shown in Fig. 2, the Si film is etched in the dark regions, and the UV light is directly incident on the BOX and, hence, on the substrate (no BOX absorption). Now, the photon flux density of $\sim 10^{13}$ photons/s $\cdot$ cm^2 generates ehp, which must diffuse to the deep-depletion region. Even if only 10% of the generated ehp is collected ($\sim 10^{12}$ ehp/s $\cdot$ cm^2), this number is on the order of or higher than the thermal generation rate, and the UV light will behave almost the same as visible light.

Since the SOI structure consists of three layers (Si film, BOX, and substrate), we also considered other possible hysteresis-inducing mechanisms, such as positive BOX charge, interface traps, and generation/recombination in the Si film. In the case of BOX charges, they can result in current hysteresis if they move with gate bias. This is unlikely, and it cannot explain the hysteresis elimination with illumination. Regarding charging and discharging of interface traps, these also cannot provide the reasons for such a large hysteresis, for example, 10 V difference in threshold voltage. The interface trap densities are extracted from the slope of the semilog plot of drain currents versus gate voltage using

$$S = 2.3 \left(\frac{kT}{q}\right) \left(1 + \frac{qD_{it} + C_{\mathrm{Si}}}{C_{\mathrm{BOX}}}\right)$$

where S is the subthreshold swing, and C_{Si} and C_{BOX} are the SOI and BOX capacitances, respectively. We obtain a D_{it} density of less than 10^{11} eV$^{-1} \cdot$ cm^{-2}, which should give a threshold voltage difference of less than 1 V, using $\Delta V_T = Q_{\mathrm{it}}/C_{\mathrm{ox}}$.

Another possibility is the Si film itself. A reverse gate voltage scan leads to higher current, meaning that the film body potential does not drop. The depletion region in the film does not shrink (as it should for negative V_G) because majority carriers are not available (for example, by the evaporated Schottky contacts). This theory, however, still does not explain the coincidence of drain current up to the kink point.

V. Simulations

We carried out simulations of the hysteresis and drain current transients with the ATLAS and ATHENA modules of SILVACO [20]. The simulated devices had a 6-μm-thick substrate, 145-nm-thick BOX, 55-nm-thick Si film, 100-μm-long source, drain, and channel each, 10^{15} cm^{-3} Si film and substrate doping concentrations, and $Q_{\mathrm{BOX}}/q = 10^{12}$ cm^{-2}. The substrate thickness was chosen for simulation mesh point density reasons. The contact work function was set at 4.33 eV. We considered concentration-dependent mobility, field-dependent mobility and the Shirahata mobility models, the Shockley–Read–Hall recombination model, bandgap narrowing, and impact ionization models for the device simulation.

Fig. 11 shows some of the transient simulation results. We considered various lifetimes for substrate and Si film in these simulations to see which has the largest influence on the hysteresis and the transient decay time. In one set of transient simulations for a *constant substrate lifetime* of 100 μs, the Si film lifetime was changed from 100 to 1 μs, and in the second set of simulations for a *constant Si film lifetime* of 100 μs, the substrate lifetime was changed from 100 to 1 μs. The substrate voltage was ramped from -10 to $+15$ V at a constant drain voltage of 0.2 V for the steady-state current–voltage simulations (not shown); for the transient simulations, the substrate voltage was ramped down from $+15$ to 0 V in 1 μs, and the transient simulation was continued for another 100 s while the substrate remained at 0 V. The steady-state I_D–V_G simulations predict the hysteresis we observe experimentally (not shown here). Fig. 11(a) shows the effect of substrate lifetime variation with constant Si film lifetime. As expected from our model, when the substrate lifetime changes, the transient time also changes. On the other hand, changes of Si film lifetime should have a smaller or negligible effect on the transient time, as is indeed shown in Fig. 11(b). These simulation results support our model of hysteresis and transients mainly controlled by the substrate. Furthermore, if the gate voltage changes from 15 V to a voltage above the kink voltage (6.5 to 7.5 V in these simulations) instead of zero, as in Fig. 11, no transient is observed—again, as predicted by our model and observed experimentally.

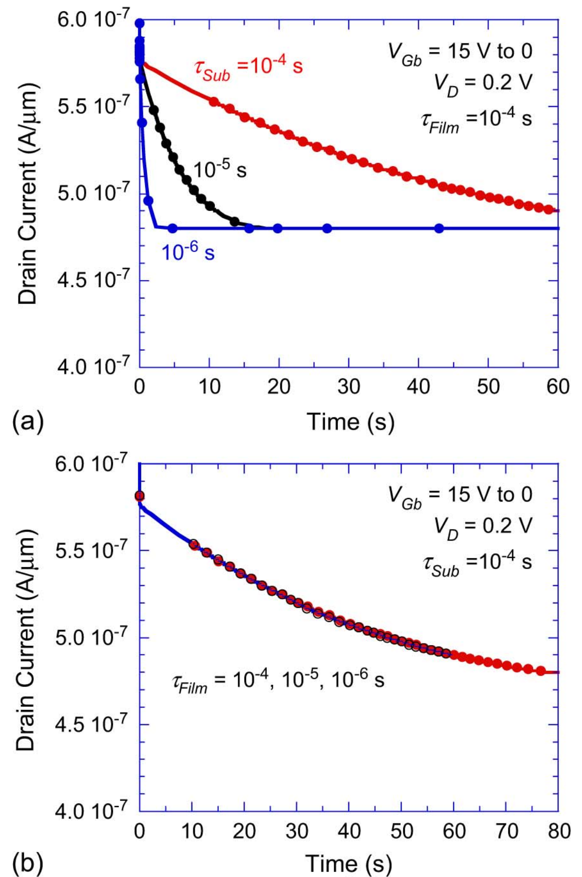

Fig. 11. Drain current versus time as a function of substrate and Si film lifetimes. (a) $\tau_{\mathrm{Si\,film}} = 10^{-4}$ s; τ_{Sub} varies. (b) $\tau_{\mathrm{Ssub}} = 10^{-4}$ s; $\tau_{\mathrm{Si\,film}}$ varies.

Fig. 5 shows the *measured* temperature dependence of the transient drain–current decay. Fig. 12 shows the normalized *simulated* drain–current transients as a function of temperature. For simplicity, the curves are normalized so that all drain currents end at the same drain current at the end of their transients.

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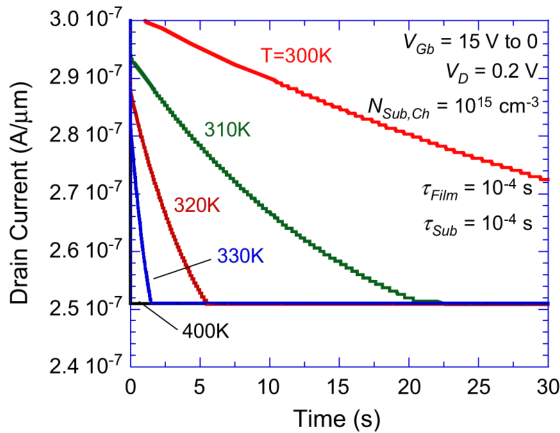

Fig. 12. Drain current versus time as a function of temperature.

The final drain currents actually differ due to temperature-dependent mobility. The substrate and film lifetimes were kept constant at 10^{-4} s for these simulations. We see that the transient time decreases as the temperature increases, which is in agreement with the experimental results, because the intrinsic carrier concentration increases with increasing temperature which increases the generation rate. As a result, the substrate depletion region vanishes rapidly, resulting in a faster transient at higher temperatures.

VI. Conclusion

Even though the Ψ-MOSFET is routinely used to characterize the quality of SOI wafers, not much attention has been paid to substrate effects on current–voltage measurement. We have observed drain current hysteresis and transient behavior during Ψ-MOSFET drain current-gate voltage measurements. Such phenomena were eliminated with illumination, elevated temperature, or low gate voltage sweep rate. A variety of measurements (static and transient drain and gate currents, transconductance, capacitance, light, and temperature) indicate that the drain current hysteresis is primarily due to substrate deep depletion rather than Si film effects. Simulations show the dependence of the transient behavior on substrate generation, confirming our experimental results and leading us to believe that our model is correct.

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