Pseudo-MOSFET Drain-Current Transients: Influence of the Substrate

Kihoon Park, Pinakpani Nayak, and Dieter K. Schroder, *Life Fellow, IEEE*

***Abstract*—The pseudo-MOSFET drain-current transient time is used to determine the generation/recombination lifetimes of SOI wafers. We have analyzed this transient for p-films on p-substrates experimentally and through simulation and show the substrate, not the Si film, to dominate this transient. For negative-substrate-voltage pulses, the substrate is driven into deep depletion, and electron–hole pair generation influences the film potential and, subsequently, the drain current.**

***Index Terms*—Drain-current transients, generation lifetime, pseudo-MOSFET, recombination lifetime, silicon.**

I. Introduction

DRAIN-CURRENT transients in SOI MOSFETs are commonly related to the floating-body. When such floating-body effects are controlled, they can be used for zero-capacitor dynamic random access memories (Z-RAMs) [1]–[8]. Retention time, related to the floating-body generation lifetime, is an important aspect of such devices. The generation lifetime, commonly determined by measuring the leakage current of p-n junctions or the recovery time of pulsed MOS capacitors (MOS-Cs), [9] can also be determined from the drain current upon pulsing the gate. The pseudo-MOSFET or Ψ-MOSFET is a simple test structure to determine a variety of Si film and film/oxide properties [10]–[13]. Since the substrate is the gate in Ψ-MOSFETs, one may expect the *substrate* and the BOX/substrate interface to play a role during the transients. For example, for p-type substrates with negative gate bias, the substrate is driven into depletion, inversion, or deep depletion, depending on whether the gate voltage is steady state or suddenly applied. As transient Ψ-MOSFET measurements are used to determine the generation and recombination parameters of the Si film, it is important to understand the substrate role during such measurements. SOI MOSFET and Ψ-MOSFET transient measurements have been used to determine generation and recombination lifetimes [14]–[25]. To our knowledge, the role of the substrate during transient measurements is rarely discussed, even though it is quite obvious that, during some of the measurements, the substrate is clearly driven into deep depletion.

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The authors are with the Department of Electrical Engineering and the Center for Solid State Electronics Research, Arizona State University, Tempe, AZ 85287-5706 USA (e-mail: parkkihoon21@yahoo.com; pnayak1@asu.edu; schroder@asu.edu).

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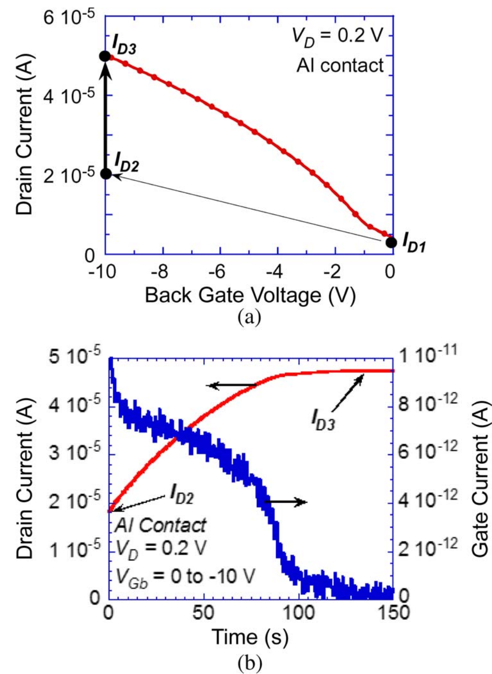

Fig. 1. Measured (a) $I_D - V_{\rm Gb}$ and (b) $I_D - t$ and $I_G - t$ characteristics for low $\phi_{\rm Bp}$.

II. Experiments

The p-film and p-substrate samples were dry oxidized at 900 °C for oxide thicknesses of 50 nm to form top gate oxides for top-gated devices. Some of the samples had top gates. After oxidation, the thicknesses were $\mathrm{SiO_2/Si/BOX} = 54/53/145$ nm. The device area was isolated from the rest of the samples to reduce possible leakage current through BOX pin holes or sample edge by etching the top thermal oxide and Si film. For the "no-top-gate" structures, the thermal oxide was etched, and 150-nm Ti/100-nm Al metal contacts were e-beam evaporated and defined by photolithography. The samples were forming gas $(5\%\ \mathrm{H_2} + 95\%\ \mathrm{N_2})$ annealed at 400 °C/20 min. Electrical measurements were made in a dark probe station at room temperature. Typical drain-current–back-gate voltage $(I_D\text{–}V_{\rm Gb})$ characteristic of a device with low hole Schottky barriers is shown in Fig. 1.

In the Ψ-MOSFET cross section in Fig. 2, consider a *negative* back-gate voltage step of $V_{\rm Gb} = -10$ V applied at $t = 0$. The drain current changes from I_{D1} to I_{D2}. The Si-film hole charge density is Q_{p2}, and the substrate space-charge-region (scr) charge density is Q_{b2}. There is very low inversion charge density Q_n. Electron–hole-pair (ehp) generation in the substrate scr proceeds. Some of the holes neutralize ionized acceptors in

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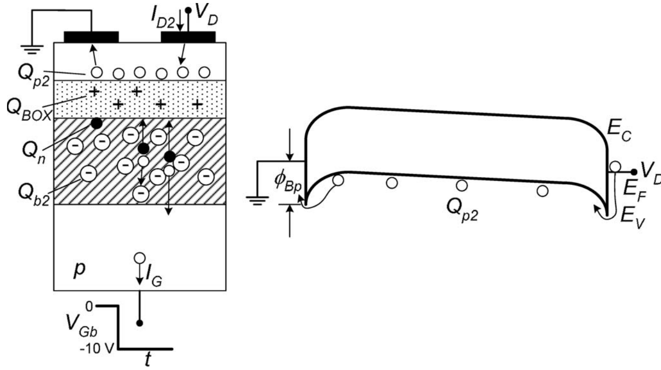

Fig. 2. Cross-sectional diagram and band diagram at $t = 0^+$.

the scr, while others leave the substrate as gate current (I_G). The holes for the $I_{D1} \Rightarrow I_{D2}$ transition are supplied by the Schottky drain contact in the band diagram in Fig. 2. The substrate inversion layer Q_n increases with time as ehps are generated in the substrate, Q_{p2} increases, and $I_D \Rightarrow I_{D3}$. For *positive* back-gate voltage pulses, the substrate is driven very quickly into accumulation and plays no role in the drain-current transient.

The reason why the substrate plays such an important role is that it changes the potential and threshold voltage of the floating Si film. As this scr collapses due to ehp generation, the voltage across it decreases, and the Si film becomes more negatively biased by capacitive coupling of V_{Gb}. If the drain-current transient is predominantly determined by substrate generation, then the gate current should have similar time dependence as is indeed observed in Fig. 1(b). The fact that the gate current flows during the drain-current transient clearly shows that substrate generation dominates the transient. If the transient were due to ehp generation in the Si film, then the gate and drain currents would be decoupled, and the gate current should be zero or negligibly low. To study the substrate generation directly, we also used the Si film islands as a gate of a MOS-C. The transient capacitance gives capacitance transient times that are very similar to the drain/gate current transient times in Fig. 1(b). In this MOS-C, the recovery is due to ehp generation in the substrate only since the Si film in this device acts merely as a gate.

III. Simulations

The I_D transient effects were simulated with ATLAS/SILVACO with device dimensions: 6-μm substrate; 145-nm BOX; 55-nm Si film; lengths of source, drain, and Si film of 100 μm; p-type Si films and substrates with $N_A = 10^{15}$ cm^{-3}; and interface charge density $N_f = 10^{11}$ cm^{-2}. Concentration- and field-dependent mobilities, Klaassen and Shirata mobility models, Shockley–Read–Hall recombination, band-gap narrowing, and impact ionization are used. V_{Gb} falls in 1 μs from 0 to -10 V and remains at -10 V for 200 s. We include a fixed sheet charge density of $Q_f/q = N_f = 10^{11}$ cm^{-2}, located in the oxide at the BOX/substrate and BOX/film interfaces, in the simulations. Fig. 3(a) shows the time-dependent drain current and the Si-film hole concentration, p_{ch}, 5 nm above the BOX/film interface and the substrate electron concentration, n_{sub}, 10 nm below the BOX/ substrate interface. The transient drain current at $t = 0$ is close to zero in this plot (it is actually $\sim 10^{-10}$ A/μm). The experimental value in Fig. 1(a) is $\sim 2 \times 10^{-5}$ A. The experimental values depend very much on the barrier heights of the device, with some devices exhibiting currents that are much lower than 2×10^{-5} A. Furthermore, the simulations are shown as current/unit width. One should not compare the actual numerical values in these plots but the overall behavior.

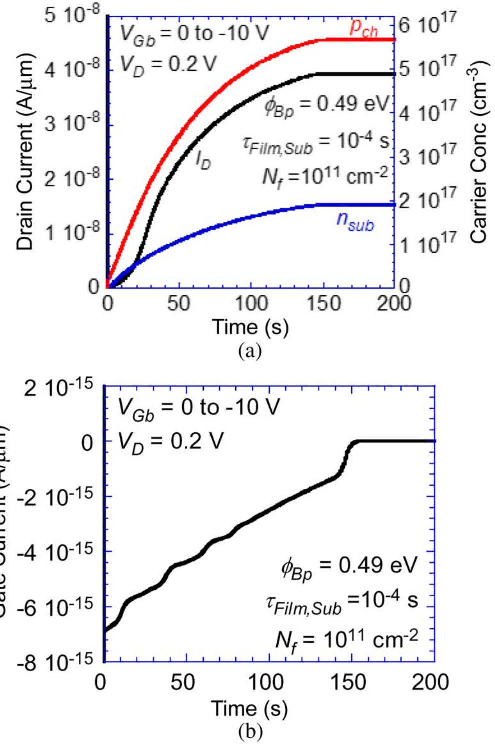

Fig. 3. Simulated (a) drain current, p_{ch}, and n_{sub} and (b) gate current versus time.

With $-V_{\mathrm{Gb}}$, the substrate enters deep depletion, and the Si film remains almost neutral. Most of the -10 V drops across the substrate scr and the BOX. The source/drain Schottky contacts are reverse biased. The higher the hole barrier height, the wider the scr. The scr at both ends of the channel creates a nonuniform hole concentration along the BOX–film interface, resulting in a hole barrier at both ends of the channel. The scr below the source contact plays a major role in controlling the drain current because the holes have to overcome this barrier from channel to ground.

The channel potential increases as the substrate scr shrinks due to ehp generation, and the drain current increases. After 140 s, the substrate ehp generation ceases (Fig. 3), creating a constant scr near the BOX/substrate interface; the substrate voltage drops; and the channel potential becomes constant. The drain current follows the hole concentration in the Si film below the source contact. Fig. 4 shows the variation of the substrate potential V_{sub} and the channel potential V_{ch} near the BOX interface with time. An important factor is the film potential (V_{film}) under the source contact near the BOX interface. This potential increases with time and saturates at the time when the ehp generation stops and I_D saturates.

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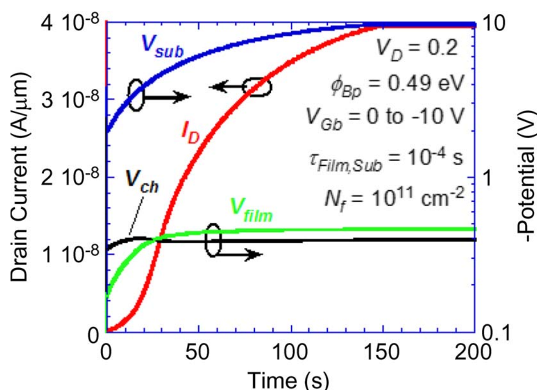

Fig. 4. I_D, $V_{\rm sub}$, $V_{\rm film}$, and $V_{\rm ch}$ versus time. The potentials are negative.

If the film plays a role in the I_D transient, then changing the carrier lifetimes in the film should affect the drain-current transient, but if the substrate controls I_D, then changing the carrier lifetimes in the substrate should affect the drain-current transient. Our simulations show that the drain-current transient time changes if we change the *substrate* carrier lifetimes, keeping the Si-film carrier lifetime constant. However, changing the *film* carrier lifetimes with constant substrate lifetime has negligible effect on the drain-current transient.

We have confined our measurements and simulations to p-films on p-substrates since most SOI wafers are of this type. As the bias conditions for accumulation, depletion, etc., are not the same, p-films on n-substrates or n-films on p-substrates will behave differently. Due to space limitations of this letter, we have not addressed these cases.

IV. Conclusion

Even though the Ψ-MOSFET is routinely used to characterize the quality of SOI wafers, not much attention has been paid to substrate behavior during transient drain-current measurements. We have carried out detailed experiments and simulations for p-films on p-substrates to show that, for negative back-gate voltage pulses, the substrate is driven into deep depletion and the drain current transient is essentially completely dominated by substrate ehp generation. For positive back-gate voltages, the substrate plays almost no role, and the transient is dominated by the Si film.

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