# Unusual $C$–$V$ Characteristics of High-Resistivity SOI Wafers

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***Abstract*—The maximum capacitance for bulk or Silicon on Insulator (SOI) wafers is governed by the gate/contact area. During our capacitance–voltage ($C$–$V$) characterization of high-resistivity SOI wafers with Al contacts directly on the Si film, we observed the maximum capacitance to be much higher than that due to the contact area, suggesting bias spreading due to the distributed transmission line of the film resistance and buried oxide capacitance. In addition, an "S"-shape $C$–$V$ plot was observed in the accumulation region.**

***Index Terms*—Bias spreading, $C$–$V$ characteristics, high-resistivity SOI (HRS), low-pass filter effect, transmission-line effect.**

## I. Introduction

HIGH-RESISTIVITY substrates exhibit lower crosstalk than low-resistivity substrates, and high-resistivity Silicon on Insulator (SOI) (HRS) substrates are yet more effective [1]. We characterized both bulk and SOI substrates and observed unusual behavior. During capacitance–voltage $C$–$V$ measurements, devices with and without a gate oxide behave very differently under certain bias conditions. The device in Fig. 1(a), consisting of a substrate that may be depleted, accumulated, or inverted (space-charge region width $W$), buried oxide (BOX) $t_{\rm BOX}$, Si film $t_{\rm film}$, and gate oxide $t_{\rm ox}$, shows conventional $C$–$V$ behavior, i.e., the capacitance depends on the gate area, which is indicated by the vertical dashed lines. However, for the device in Fig. 1(b) with a metal contact directly on the Si film without a gate oxide, the capacitance can be governed by an area significantly larger than the gate area. How can this be?

Our simulations and measurements show that, if the film is accumulated, the effective area can extend beyond the gate area. This effective area depends on frequency $f$ of the ac signal. Fig. 1(b) shows such a case, where the film is represented by resistance $R$, and the BOX and the underlying substrate are represented by capacitance $C$ as a distributed transmission line, and the distance for the ac signal to laterally propagate depends on $f$, $R$, and $C$. It is this lateral distance, which is indicated by the gray arrows, that determines the effective gate area that varies with frequency and depends on whether the film is accumulated, depleted, or inverted. Bulk substrates do not exhibit this unusual behavior.

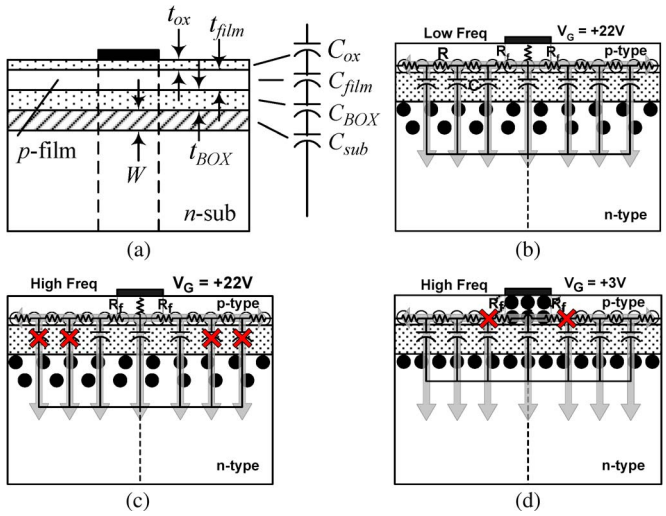


Fig. 1. SOI wafers (a) with and (b) without a gate oxide. (b) At low frequency, the ac signal spreads further. (c) At very high frequencies due to the low-pass filter nature of the $RC$ network, the ac signal remains closer to the contact area. (d) At high frequency and low positive bias, the depletion region separates the accumulation and the inversion region, reducing the spreading.

We should mention that MOS capacitors on high-resistivity substrates also do not behave in the same way as those on low-resistivity substrates due to the substrate potential drop and the longer Debye length [2]. Furthermore, low-frequency MOS $C$–$V$ behavior is observed at higher frequencies due to shorter response time $t_r = (N_A/n_i)\tau_g$ since $N_A$ is very low. Minority inversion carriers follow the ac signal provided that the period of the ac signal is much longer than the response time. For example, for $N_A = 10^{16}$ cm$^{-3}$, $n_i = 10^{10}$ cm$^{-3}$, and $\tau_g = 1$ ms $\Rightarrow t_r = 1000$ s, whereas for $N_A = 10^{12}$ cm$^{-3}$ $\Rightarrow$ $t_r = 0.1$ s. The MOS-$C$ frequency response is proportional to $1/t_r$, leading to low-frequency behavior for frequencies as high as 1 kHz (see Fig. 4).

## II. Experiments and Simulations

$C$–$V$ measurements were made using HP4284 on various unibond HRS wafers with aluminum contacts of different areas at 100 kHz with *substrate* dc bias to suppress noise. Series of $C$–$V$ measurements were used as they are more accurate for high-resistivity samples. Our samples had doping concentrations $< 5 \times 10^{12}$ cm$^{-3}$. Oxygen is incorporated into the growing silicon ingot from the quartz crucible; the oxygen forms thermal donors under certain anneal conditions, and at

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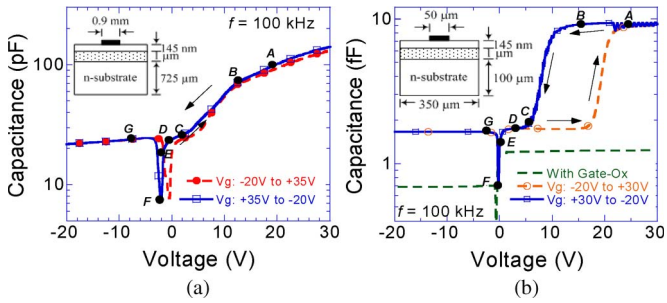


Fig. 2. (a) Experimental and (b) simulated $C$–$V$ plots with and without a gate oxide for an HRS wafer. Capacitance after 10 V is much higher than that due to the contact area at point D, indicating bias spreading.

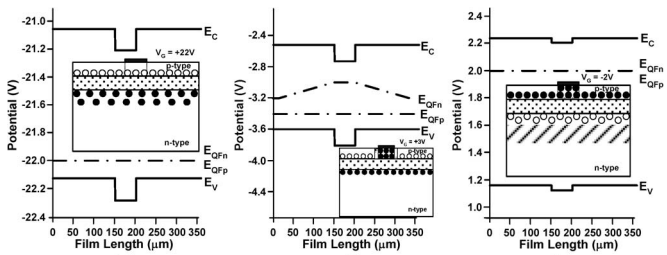


Fig. 3. Device cross section and energy band diagrams in the film 15 nm above the film/BOX interface. (a) At +22 V, point A in Fig. 2, the entire film and the substrate interface is completely accumulated (charge spreading). (b) At +3 V, point D in Fig. 2, only the film below the contact is inverted, the rest are partially accumulated, the substrate is accumulated, and the Fermi level splits due to minority carrier injection from the Schottky contact. (c) At −2 V, point G in Fig. 2, the entire film and the substrate interface is completely inverted (charge spreading).

such low doping concentrations, the oxygen thermal donors converted the p-type substrate into an n-type [3]–[5], as shown by the simulations comparing p- and n-type substrates. Only when the substrate is a lightly doped n-type and the film is a p-type do the simulations match the experimental results. In these samples, as the film has a higher doping concentration than the substrate, the thermal donors can easily convert the substrate into an n-type than the film.

Fig. 2(a) and (b) shows the experimental and simulated $C$–$V$ plots with the device cross sections in the insets. The *experimental* results in Fig. 2(a) were measured at 100 kHz; the gates are 0.9-mm-diameter aluminum dots on the silicon film of an SOI wafer with a 145-nm-thick Si film, a 1-$\mu$m-thick BOX, and a 725-$\mu$m-thick substrate. The substrate is 8 × 4 cm. The corresponding *simulated* plots in Fig. 2(b) are for a wafer with a 145-nm-thick Si film, a 1-$\mu$m-thick BOX, a 350-$\mu$m-wide and 100-$\mu$m-thick substrate, a $10^{14}$ cm$^{-3}$ p-type film, and $7 \times 10^{11}$ cm$^{-3}$ n-type substrate doping densities (the doping densities were chosen to match the simulated and the experimental results). A Silvaco ATLAS 2-D device simulator was used.

The work-function difference between the Al contact and the p-type silicon film is $\Phi_{\rm MS} = -0.77$ eV, and between the n-type silicon substrate and the Al contact, $\Phi_{\rm MS} = -0.42$ eV. This creates a high hole and a very low electron barrier height, allowing minority electron injection into the film and causing the film below the contact to invert and the region away from the contact to deplete. The film below the contact is a source of minority carriers affecting $C$–$V$ at higher frequencies.

To explain the behavior of $C$–$V$ plots, some of the critical bias points are marked in the experimental/simulation results in Fig. 2. With the contact directly on the film, the bias is no longer confined to the contact area but spreads to a larger area in the film due to direct coupling between the film and the contact. At higher positive bias, the entire p-type film, including the film/BOX interface, is accumulated with holes, and the n-type substrate/BOX interface is accumulated with electrons [see point A in Fig. 2 and 22 V in Fig. 3(a)]. As the film is completely accumulated, there is no minority carrier injection. The continuous sheet of holes provides a conducting path to the ac signal that spreads through this layer limited by the layer sheet resistance. Due to this spreading, the measured capacitance is the total capacitance spread along the BOX area, which is much larger than the contact area. *The spreading is frequency and bias dependent and controlled by the low-pass filter behavior of the RC network of film/BOX/substrate interfaces* in Fig. 1(b)–(d).

This spreading effect is also confirmed by calculating the effective area from the measured capacitance. The capacitance at point A (22 V) at 110 pF is much higher than that for a contact diameter of 0.9 mm. The area from the measured capacitance at "A" is more than five times larger than the contact area. A similar increment is observed in the simulation. The extent of spreading also depends on the contact size and the frequency of the ac signal for a particular dc bias. In the simulation, the capacitance saturates at higher positive bias, whereas in the experiments, it has a shallow rising slope, which is mainly due to the fixed substrate width of 350 $\mu$m in the simulation. The charges tend to saturate within this area after a certain bias, whereas in the experiment, the sample size is much larger than the contact size, and therefore, the spreading continues to increase with bias.

With reduced bias, the holes try to leave the film, but they face a high hole barrier Schottky contact. This effect is predominant at lower positive biases. At around 12 V (see point B in Fig. 2), the film below the contact begins to deplete/invert due to the Schottky contact [see Fig. 3(b)], and the inverted region below the contact is separated from the accumulated region of the film by a depletion region. This depletion region acts as a large resistor $R_f$ connecting the contact region of the film to the lateral region [see Fig. 1(d)]. $R_f$ increases as positive bias reduces, the coupling to the lateral region is reduced, and the ac signal is confined closer to the contact; hence, the spreading reduces, and the measured capacitance gradually reduces to the contact area capacitance [see Fig. 1(d)]. More and more carriers below the contact area begin to respond (the film below the Schottky contact acts as a source of minority electrons) compared with other parts of the still accumulated film. The formation of the depletion region at low positive bias leads to lower spreading and minority electrons only below the contact responding to the ac signal results in a capacitance change from a high (similar to the spread area) to a low value (similar to the contact area) along the "S"-shape (see point B to C). For bias $< 5$ V, the capacitance corresponds to that of the contact area [see point D in Figs. 2 and 3(b)].

At a negative bias close to zero, the substrate is completely depleted. The depletion region is much wider than the BOX thickness, and the capacitance reaches its minimum value (see point F in Fig. 2). With further negative bias, the film inverts within few 100 mV after the minimum capacitance (see point G

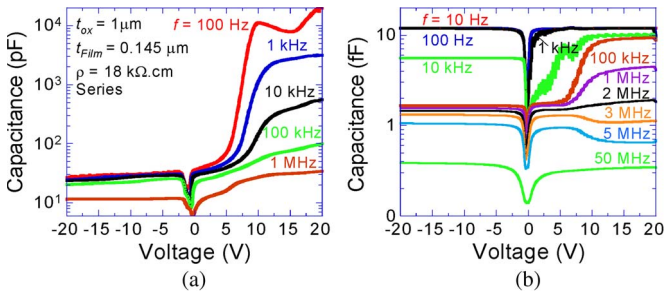


Fig. 4. SOI $C$–$V$ effect of frequency. (a) Experimental. (b) Simulation.

in Fig. 2). Unlike accumulation with a discontinuity of charges under and away from the contact, in inversion, there is a continuous layer of electrons in the film all along due to the negative bias and the Schottky contact [see Fig. 3(c)]. Simultaneously, the substrate/BOX interface is also inverted with holes. In the film, although the minority electrons can be easily supplied by the contact, the minority holes in the substrate have to be thermally generated, and the substrate inversion layer cannot respond to the higher frequency, and the capacitance saturates at a value corresponding to the substrate depletion capacitance. The inversion layer spreads all along the BOX interface in the film and the substrate. Due to spreading, the inversion capacitance is higher than the minimum depletion capacitance at point F.

For the positive-to-negative sweep direction [see Fig. 2(a) and (b), bold line], holes accumulated in the film during the initial high positive bias cannot move out of the film easily when the bias becomes less positive due to the high hole barrier. The accumulated holes create a higher positive potential in the film and prevent the film potential from reducing in response to the reduction in applied bias; a lower positive bias is required to drain the holes and reduce the capacitance. In the negative-to-positive sweep direction [see Fig. 2(a) and (b), dotted line], there are no accumulated holes in the film as the film is inverted. It takes a higher positive bias compared with the previous sweep direction to build up enough holes along the BOX/film interface, leading to a hysteresis-like behavior.

The frequency response of the $C$–$V$ plot is controlled by the $RC$ network [see Fig. 1(b) and (c)]. Hence, at low frequencies for positive and negative biases, the ac signal can spread further so that the charges in the film under and away from the contact and the corresponding substrate charges can respond. Hence, we observe higher low-frequency capacitance than high frequency at all biases [see Figs. 1(b) and 4]. With increasing frequency, the ac signal travels closer to the contact due to lower capacitive reactances. It spreads less into the film, leading to lower capacitance values [see Fig. 1(c)]. The "S"-shape remains for positive bias. In the simulation, for $f < 1$ kHz, both inversion and accumulation capacitance values are the same and are the spread values (see Fig. 4).

At very high frequencies, the "S"-shape in positive bias vanishes as almost all of the ac signal flows very close to the contact area, i.e., beyond 2 MHz in Fig. 4(b). With a further increase in frequency, the capacitance values at all biases (including the minimum capacitance) reduce as the substrate resistance of an HRS wafer becomes more important. Nicollian and Goetzberger [6] observed bias spreading and focused on the $RC$ behavior in the inversion region; in our case, the $RC$ behavior and its effect on capacitance is in both accumulation and inversion regions with no lateral source of minority carriers.

As the contact area increases, the capacitance increases due to the larger contact area and corresponding increase in spreading. Our simulations and experiments show that the increase in the spreading effect is not always proportional to the contact area. As the contact area increases, the ratio of spread area/contact area for smaller contacts is much larger than that for larger contacts. In the simulation, we observed reduced capacitance, i.e., spreading, when the substrate length is reduced for a fixed contact length, confirming the spreading theory. Figures are not shown.

With a gate oxide on the Si film, this capacitance anomaly is not observed [see Fig. 2(b)]. Previous experimental results did not show any spreading effect with a gate oxide on SOI samples either [7]. Spreading was observed for thin ($t_{\rm film} = 145$ nm) and thick ($t_{\rm film} = 1.25\ \mu$m) SOIs in both the simulation and the experiment, but the "S"-shape was absent in the thick-film SOI. For the p-type film and n-type substrate combination with the Al contact directly on the film, an n-type $C$–$V$ curve is observed for both thick- and thin-film SOIs in both the simulation and the experiment. However, when the Al contact is placed over a gate oxide, then for the same combination of film and substrate doping, the thin-film SOI shows an n-type $C$–$V$ curve, whereas the thick-film SOI shows a p-type $C$–$V$ curve in both the simulation and the experiment. In thick films, the film depletion layer may not touch the interface, thereby dominating $C$–$V$.

The main point of this letter is to be aware of SOI characterization, which, under certain conditions, leads to erroneous results, and to understand the related $C$–$V$ behaviors. In summary, HRS samples with an Al contact directly on the Si film show bias spreading to an area much larger than the contact area and a corresponding increase in capacitance, but not when there is a gate oxide. The $C$–$V$ plots also showed an "S"-shape behavior in the accumulation region mainly due to the Schottky contact with high hole barrier heights that create a discontinuity in the accumulation layer in the film by depleting/inverting the film below the contact. The low-pass filter effect of the $RC$ transmission line of the film/BOX/substrate interfaces plays a significant role in bias spreading and increased capacitance by controlling the area through which the ac signal flows.

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