Improvement in gate oxide integrity on thin-film silicon-on-insulator substrates by lateral gettering

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Lateral gettering is implemented in thin-film silicon-on-insulator (TFSOI) substrates by introducing crystalline defects in the vicinity of metal-oxide-semiconductor device channel regions prior to gate oxidation. As a result of the gettering a significant improvement in gate oxide integrity is achieved, with increased oxide breakdown voltages and charge-to-breakdowns, as well as a reduction in localized oxide charge trapping. The same gettering effect on separation-by-implantation-of-oxygen and bonded silicon-on-insulator substrates suggests that the lack of effective gettering is mainly responsible for the oxide degradation regardless of the TFSOI type. This work also demonstrates the feasibility of achieving bulk-comparable gate oxides on TFSOI substrates. © *1997 American Institute of Physics.* [S0003-6951(97)03249-X]

The presence of metallic contaminants is known to have a negative impact on the performance of electronic devices by introducing generation–recombination centers within the band gap, leading to an increase in the leakage current and a reduction of the minority carrier lifetime. Furthermore, crystalline defects when decorated with metals can degrade the gate oxide quality.[1] One way to avoid these problems is to remove the impurities from the device active regions by gettering. Great success has been achieved in impurity gettering in Si wafers,[2] with the formation of either oxygen precipitates as intrinsic gettering or backside defects as extrinsic gettering. The standard gettering techniques, however, are not effective for thin-film silicon-on-insulator (TFSOI) substrates due to the presence of a buried oxide, which tends to prevent the movement of slow diffusers from the top TFSOI layer into the bulk substrate at 1000 °C or below.[3,4] This implies that, under standard thermal conditions for device processing, impurities introduced during the process may remain in the active area. It was reported that gate oxide integrity (GOI) on TFSOI was strongly area dependent[5,6] indicating the existence of high defect densities. However, grown-in dislocations and surface micro-roughness were not considered as primary causes of early oxide failures.[5] It is therefore necessary to investigate gettering effects on TFSOI.

Impurity gettering in TFSOI wafers has received some attention in the past, but most of the reported gettering techniques still involve the diffusion of impurities from the TFSOI wafer surface to either the bottom of the buried oxide[3,4,7] or to a backside defect region.[8] To overcome the limitation of impurity gettering in TFSOI, the gettering sinks should be placed in the TFSOI layer rather than in the Si substrate. By demonstrating the effectiveness on Schottky diodes, a lateral gettering technique was proposed by researchers at North Carolina State University (NCSU)[9] for metal-oxide-semiconductor (MOS) devices on TFSOI. They suggested forming gettering sinks adjacent to MOS device channel regions by ion implantation and subsequent heat treatment after gate formation, while the gate was used to mask the implant flux in the device channel region. We believe that this approach is very useful for diodes on TFSOI, but post-gate gettering may not be efficient for GOI improvement. For *n*-type MOS (NMOS) devices fabricated on TFSOI, the source-drain (S/D) phosphorus implant followed by dopant activation is expected to leave implant damage such as dislocations to serve as effective gettering sinks. As a part of our standard process flow the S/D implants are performed on all MOS capacitors fabricated on TFSOI. Had the post-gate gettering technique been effective, much better GOI would have been achieved in our early studies.[5] In this letter we demonstrate a significant improvement in GOI on TFSOI using a more effective lateral gettering technique. This work supports the basic idea of lateral gettering proposed by the NCSU group, while the gettering scheme is modified to meet the need of GOI improvement.

As illustrated in Fig. 1 crystalline defects were introduced in TFSOI by a Si implant, through photo mask openings and a 150 nm sacrificial oxide (SacOx), prior to gate oxidation. The typical Si implant was performed at 135–175 keV with a dose of mid-$10^{15}/cm^2$. Under such conditions the 100 nm TFSOI layer was completely amorphized in the implant regions and recrystallization in the vertical direction was prohibited due to the lack of a crystal seed layer at the bottom of the TFSOI layer. At an elevated temperature lateral regrowth originating from the surrounding undamaged area left crystalline defects in the center of the implant regions, which served as gettering sinks for local impurities.

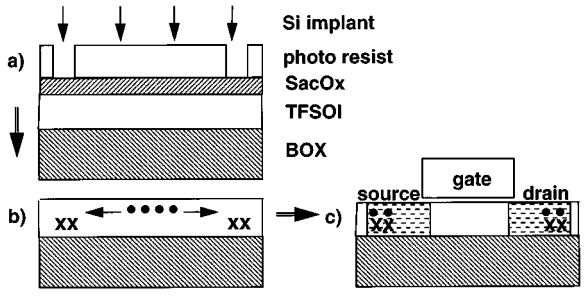

FIG. 1. Schematic diagram showing the fabrication of MOS devices with lateral gettering; (a) localized amorphization of TFSOI by Si implant, (b) heat treatment to form crystalline defects (xxx) and allow impurities (•••) to be gettered, and (c) gate oxide growth and MOS device fabrication with the crystalline defects and impurities away from channel region.

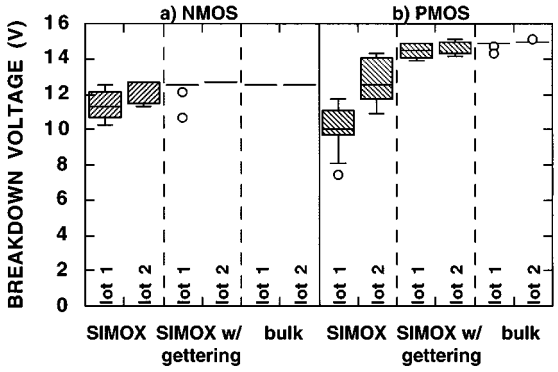

FIG. 2. Box plot of ramp-voltage breakdown on (a) NMOS and (b) PMOS capacitors with and without lateral gettering. Results in two lots are shown. The capacitor area is 3.3×10^{-3} cm^2.

The defects could (but do not have to) be located in the future S/D regions, so long as they are not at the gate edge to avoid possible leaky junctions and impaired oxides. With no special thermal process added in this work, the formation of gettering sinks and the removal of unwanted impurities were actually realized during temperature ramp-up (from 750 to 900 °C) and stabilization (at 900 °C) in an oxidation furnace before gate oxide growth at 900 °C. MOS capacitors with a 10.5 nm thermal oxide were fabricated, as a part of the standard complementary metal oxide semiconductor process flow,[10] on TFSOI substrates with and without the gettering implant. The capacitors are exactly the same as standard MOS transistors except with a tied S/D. For comparison, MOS capacitors were also built on unimplanted bulk Si substrates under the same process conditions.

The quality of gate oxides was characterized with ramp–voltage breakdown, step-current charge-to-breakdown (QBD), and Fowler–Nordheim (F-N) current–voltage ($I-V$) measurements. On both NMOS and p-type MOS (PMOS) capacitors, the gate voltage was applied between the gate and the tied S/D with the SOI in inversion. For the ramp-voltage breakdown test, the breakdown criterion was defined as a current density of 300 mA/cm^2. The size of the capacitors used in this work is 3.3×10^{-3} cm^2.

Figure 2 presents the box plot of ramp-voltage breakdown of NMOS and PMOS capacitors built on separation-by-implantation-of-oxygen (SIMOX) substrates with and without gettering. Two lots shown here were run separately but with the same process flow. As a result of gettering, the average breakdown voltages (BV) of both the NMOS and PMOS capacitors are improved with much tighter breakdown distributions. The improved BVs are very close to the bulk values. It is worth noticing that with no gettering the quality of gate oxides on SIMOX varies from lot to lot due to its high sensitivity to small variations in material and/or process conditions, whereas the oxide becomes more robust with gettering. Although the same breakdown criterion is used to characterize both NMOS and PMOS capacitors, BVs are 2 V higher on the PMOS capacitor than on the NMOS ones. This is due to the electron tunneling predominately from the valence band of a p^+ gate in the case of PMOS gate injection,[11] which results in a shift in PMOS $I-V$ curves with respect to NMOS curves.

The cumulative QBD plot in Fig. 3 reveals the same

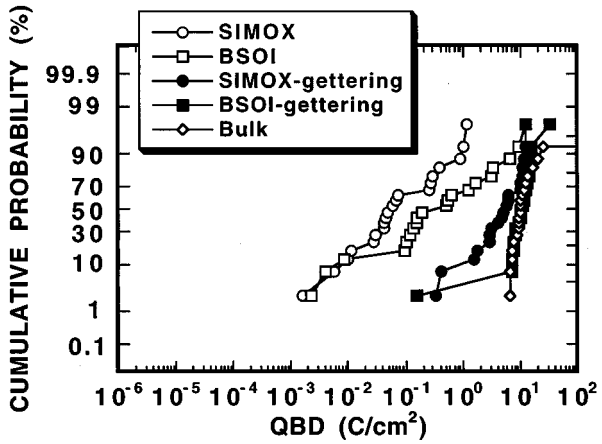

FIG. 3. Cumulative probability plot revealing the gettering-induced QBD improvement for NMOS capacitors on SIMOX and BSOI substrates. The capacitor area is 3.3×10^{-3} cm^2.

gettering effect on SIMOX and bonded SOI (BSOI) wafers. With impurity gettering, the percentage of QBDs greater than 1 C/cm^2 increases from 10%–30% to 90%–95% on TFSOI substrates. Similar gate oxide qualities on SIMOX and BSOI were reported in our early study.[5] The current work further demonstrates the same first-order mechanism of oxide degradation regardless of the TFSOI type.

Lateral gettering leads to not only a significant increase in breakdown voltage but also the elimination of $I-V$ humps present in the case of no gettering (Fig. 4). According to early studies the humps appeared during both substrate injection[5] and gate injection,[12] regardless of the doping type or perimeter-to-area ratio of the gate.[12] Reduced or eliminated upon subsequent voltage sweeps, they were attributed to the existence of positively charged traps (or positive charges) in the oxide.[5,12] The oxide charge trapping was further investigated with capacitance-voltage (C-V) measurements and the detailed results will be presented elsewhere. In brief, high- and low-frequency C-V curves were exactly identical for SIMOX capacitors with and without gettering, suggesting no measurable difference in either densities of interface state or oxide trapped charges in the as-fabricated capacitors. To study the field-induced charge generation that usually occurs during F-N $I-V$ measurements,[13] flatband

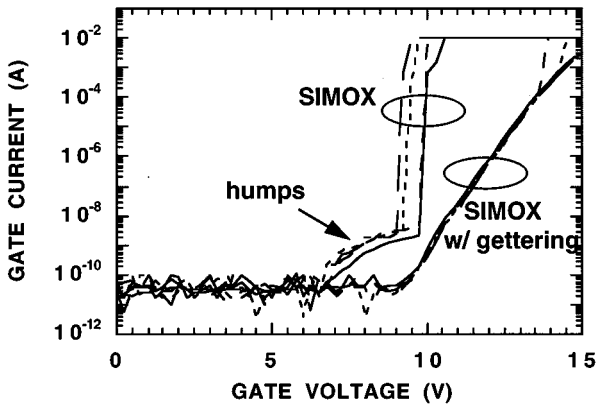

FIG. 4. Plot of gate current vs. gate voltage showing the elimination of $I-V$ humps on PMOS capacitors as a result of lateral gettering. The capacitor area is 3.3×10^{-3} cm^2.

voltage shifts were monitored under various room-temperature gate-current-stress conditions (i.e., gate or substrate injection with current densities from 10^{-7} to 10^{-5} A/cm^2). Some of the no-gettering capacitors did not survive high-field high-fluence gate stressing, but prior to the oxide breakdown flatband voltage changes were essentially the same with and without gettering.

Based on the above results, the oxide charge trapping observed in Fig. 4 is highly localized and thus undetectable by the C-V measurements. This is because the C-V characteristics determined by displacement currents often reveal average oxide qualities, whereas the $I-V$ results are dominated by weak spots in an oxide.

The reduction of localized charge trapping by lateral gettering suggests a possible correlation with the existence of metallic impurities. In fact, some metals such as aluminum are known to form electron traps in bulk oxides.[14–16] Metallic contaminants in starting TFSOI materials and introduced during device processing were investigated at various process steps up to gate oxidation, on unpatterned wafers (without gettering). At all these steps the metal concentrations were close to or below the detection limits of conventional total reflection x-ray fluorescence (TXRF) and secondary ion mass spectrometry (SIMS). By using synchrotron radiation induced TXRF and vapor phase decomposition inductively coupled plasma–mass spectrometry (VPD ICP-MS) with improved detection limits, most transition metals (Cr, Fe, Co, Ni, Cu, and Zn) found in the gate oxide were at low 10^9/cm^2 levels while the Ti concentration was between mid 10^9/cm^2 and 1×10^{10}/cm^2. Although such low level impurities are usually acceptable for standard Si processing, whether they are an issue for TFSOI is still a question (especially when they are nonuniformly distributed due to the existence of microdefects or stresses). In addition to the transition metals, aluminum at low to mid 10^{10}/cm^2 level was revealed by the VPD ICP-MS. The Al contamination present prior to gate oxidation, even at low 10^{10}/cm^2 levels, was reported to correlate with electron trapping in the oxide.[14] Although a reduced Al concentration is expected in the case of gettering, it is difficult to verify with either VPD ICP-MS or TXRF, as the former can only be applied to unpatterned wafers and the latter is not sensitive to Al.

It is noted that with deep level transient spectroscopy (DLTS) on Schottky diodes, the NCSU group demonstrated a reduced Fe concentration in the active area by introducing crystalline defects in the adjacent regions.[8] Although not on MOS capacitors, their work undoubtedly supports the effectiveness of lateral impurity gettering. The improvement in GOI presented in this work favors the basic idea of lateral gettering, while the gettering scheme is modified for GOI improvement. Our major modification includes the incorporation of gettering activities prior to gate oxidation as opposed to after the poly-Si gate formation. It is important that the unwanted impurities be removed before gate oxidation, as the quality of starting Si has a direct impact on the grown oxide. In a separate study, we also investigated the effect of the post-gate gettering but with no improvement in GOI. On the other hand, the gettering implant in this work was performed through a mask, which located implant damage far from device channel regions and therefore minimized the possibility of oxide degradation or junction leakage.

In addition to metallic impurities, this work does not rule out the possibility of gettering point defects or microdefects in MOS device channel regions. The point defects, such as vacancies, interstitials, recoiled oxygen due to through-oxide implantation, etc. could possibly induce the formation of other oxide killing defects.[17,18] To unambiguously identify the impurities or defects removed by lateral gettering in a specific TFSOI material or device process, further investigations in this area with techniques such as DLTS or the position annihilation method[19] will be necessary.

In conclusion, a primary cause for the degradation of gate oxides on both SIMOX and BSOI is the lack of effective gettering. Significant GOI improvements for TFSOI capacitors have been achieved by implementing lateral gettering sinks prior to gate oxide growth. With continuing TFSOI material and process developments, as well as further improvements in gettering, it is feasible to achieve bulk-comparable gate oxides on TFSOI.

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