Leakage current models of thin film silicon-on-insulator devices

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(Received 29 August 1997; accepted for publication 8 January 1998)

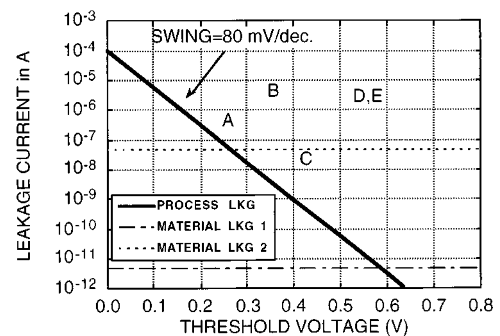
Thin film silicon-on-insulator (SOI) devices have an advantage of excellent isolation due to the buried oxide layer leading to reduced capacitance coupling and no latchup in complementary metal-oxide-silicon circuits compared with bulk silicon devices. Reduced junction area should lead to lower leakage for a given device. However, because of the buried oxide, stress is built up in the Si island during isolation processes, especially near the island edges, inducing new kinds of leakage currents, which are not observed in bulk silicon devices. This letter proposes five leakage current models of the partially depleted SOI devices, identifies their origins, and suggests methods to prevent each type. © *1998 American Institute of Physics.* [S0003-6951(98)01510-0]

Thin film silicon-on-insulator (SOI) complementary metal–oxide–silicon (CMOS) technology has long been demonstrated to show advantages over its bulk silicon counterpart in speed, power dissipation, short channel effect, latchup immunity, and reduction in process complexity and steps.[1] The additional buried oxide (BOX), less than 400 nm, enhances isolation between devices and requires no field implantation. However, because of the rigid BOX layer, Si islands are vulnerable to stress buildup at the edges. For example, high stress at edges, caused during field oxidation, enhances boron diffusion in n-type metal–oxide–silicon (NMOS) devices and introduces new kinds of leakage current mechanisms in SOI devices.[2] This letter proposes leakage models of the partially depleted SOI devices for both NMOS and p-type MOS (PMOS) and discusses their mechanisms.

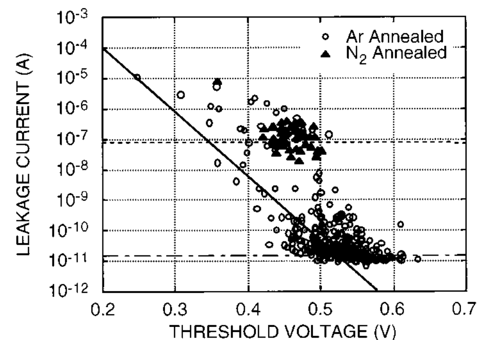
All devices measured were fully processed with conventional SOI flows with polybuffered local oxidation of silicon (PBL) isolation, as published previously.[2] Target device sizes were 25×0.6 and 0.6×0.6 μm^2 in the active regions. Drain current-gate bias (I_d-V_g) measurements done at a varying drain bias (V_d) both on an automatic tester and a handprobe tester were used as major characterization tools.

The leakage current mechanism models of partially depleted SOI devices fall into the following five types; (A) low threshold voltage (V_t), (B) punchthrough effect, (C) n-type back channel effect, (D) defect-induced leakage, and (E) edge-induced hump-type leakage. However, more than one leakage type was observed in many of the actually leaky devices.

To identify the leakage mechanisms more efficiently, a new kind of plot, called the "I_{dss} (I_d at $V_g=0$ V and V_d $=1.8$ V)-V_t plot," was devised. This is an expanded box-and-whisker plot of log(I_{dss}) along the axis of V_t, which was determined using the linear extrapolation method from maximum transconductance.[3] Figure 1(a) is a theoretical example of such a plot with the inscription of the five corresponding regions along with three boundaries of possible leakage sources. The process leakage line (solid line) is a boundary with the same sub-V_t swing [80 mV/dec in Fig. 1(a)] but different V_t's, which corresponds to type A. If the swing increases, the slope decreases. The intercept point of this line at $V_t=0$ is roughly the I_d at V_t, but no physical meaning should be assigned. This line shifts in either direction depending on the device size. The lower material leakage line 1 is the normal drain junction leakage current which varies depending on the SOI wafer types or the current detection limit of the testing tool. The upper material leakage line 2 is a special case of line 1 corresponding to type C with high



(a)



(b)

FIG. 1. (a) A schematic plot of I_{dss} vs V_t with five indicated regions of leakage sources and boundaries and (b) an example of such with data points of two types of substrates with three leakage boundaries.

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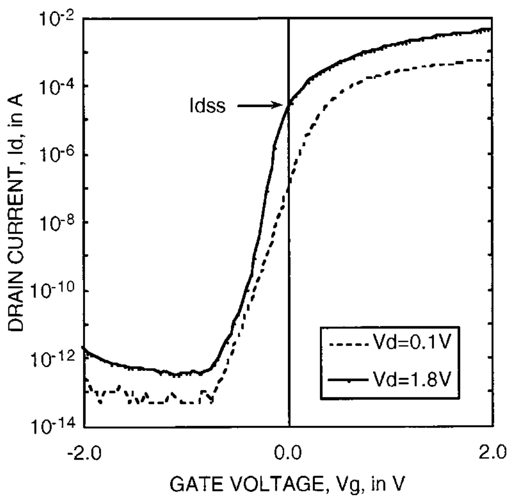
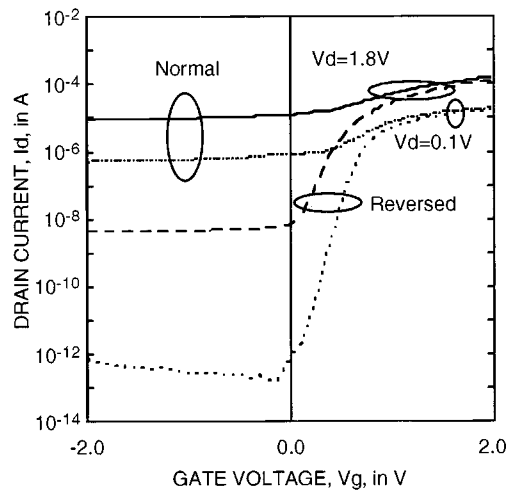


(a)



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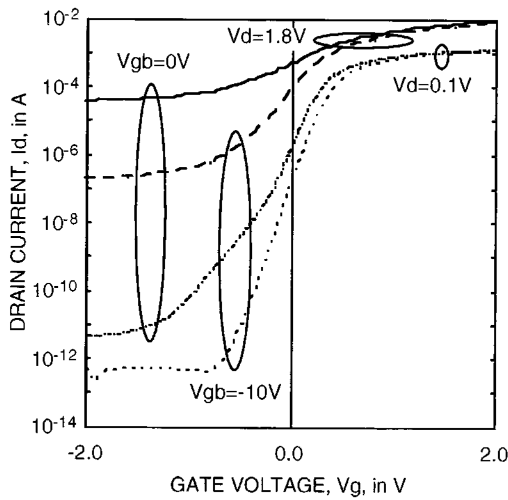

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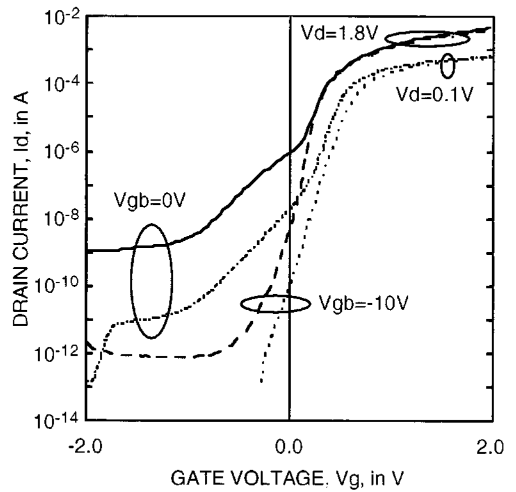
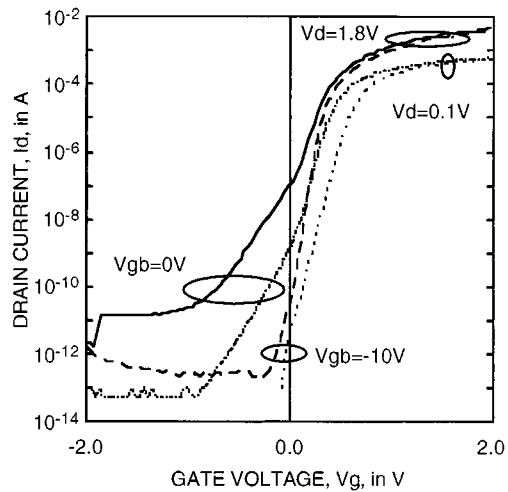


(e)



(c)

FIG. 2. Five typical $I_d - V_g$ patterns of NMOS devices with leakage mechanisms of (a) low V_t, (b) punchthrough, (c) n-type back channel, (d) defect, and (e) edge hump.

junction leakage current. Since types D and E overlap, subsequent $I_d - V_g$ measurements are required to differentiate them. An example is shown in Fig. 1(b) obtained from two different types of materials with the three leakage boundaries. The open circles are from electrically damaged wafers and most of the leakage high fliers ($I_{dss} \gg 10^{-8}$ A) are type A while the filled triangles are type C to be discussed in detail later. Examples of $I_d - V_g$ characteristics of these five leakage models are shown in Figs. 2(a)–2(e).

Type A is due to low V_t. Low doping concentration is a major reason. Since the sub-V_t swing does not change, the entire $I_d - V_g$ curve shifts to lower V_g exhibiting more leakage as V_t decreases. Higher doping concentration remedies the problem by increasing V_t. It was found that the hole

trapping (its source is unknown) in the gate oxide of NMOS devices is another reason even though it shows similar $I_d - V_g$ curves but unreasonably lower V_t than the expected one from the doping concentration. Most of the leakage current of Ar-annealed wafers shown in Fig. 1(b) were caused by this reason. It was completely eliminated by slight electron injection with $\lesssim 8$ V stress to the gate. However, higher stressing increased V_t due to electron injection.

Type B is a punchthrough effect due to the short channel length or nonuniformly lower doping concentration at the Si/BOX interface. Punchthrough leakage increases with increasing V_d due to a wider depletion region. Unlike bulk Si devices, back gate bias (V_{gb}) decreases this leakage by attracting majority carriers to the Si/BOX interface reducing the depletion region. However, if punchthrough is severe such as in very short channel devices, V_{gb} is not effective. V_t varies widely depending on the amount of punchthrough. This occurs due to process issues such as shorter than normal gate length or nonuniform doping concentration.

Type C is due to an additional n-type back channel on NMOS devices, especially built on N_2-annealed separation by implantation of oxygen (SIMOX) wafers.[4,5] NMOS V_t decreases because of lower acceptor concentration while PMOS V_t increases since the effective donor concentration increases. PMOS devices never have type C leakage on N_2-annealed wafers. Negative V_{gb} eliminates the n-type back channel and robust devices can be obtained. As an alternate, heavy p-type doping preferentially at the BOX interface can suppress it, but dose optimization should be made not to increase channel V_t.

Type D is a defect-induced leakage, which is unique in SOI devices. Defects such as threading dislocations (no dislocation loops[6,7]), which happen to locate across the drain junction region and are decorated by dopants, form a secondary $p^+ - n^+$ junction and induce extra leakage paths. The defects are either intrinsic in the starting wafers (high-dose SIMOX wafers have more defects than bonded wafers) or extrinsic from the processes such as field and sacrificial oxidation and source/drain implantation. However, it is believed that dopant diffusion to dislocations must take place, which is strongly governed by stress distribution in the silicon islands. The threading dislocations near the source and drain are not always the leakage sources as shown by transmission electron microscopy (TEM) and electrical device analyses.[8] If the source and drain are reversed for these types of leaky devices, the leakage current is reduced, as shown in Fig. 2(d). Similarly the reverse is possible. V_{gb} does not reduce this defect-induced leakage current, which distinguishes it from severe punchthrough leakage. Interestingly, type D is more dominant in NMOS devices than in PMOS devices because boron diffuses faster than phosphorus. Therefore, both the defect density of the starting wafers and low stress processes are important. Sometimes V_t was found to be very low, but this is because the linear extrapolation method[3] is not applicable to the Fig. 2(d) like device.

Type E is edge-induced hump-type leakage which is most frequently and unique on SOI devices. The $I_d - V_g$ pattern in Fig. 2(e) is an overlay of two regions from the main channels and edges. Thus Na decreases at the edge, lowering V_t locally and boron depletion generates an n-type channel at the edges. In NMOS devices tensile stress buildup near the Si island edge causes boron atoms to diffuse into the nearby oxides. An $I_d - V_g$ curve superimposed from the edge shifts to a lower V_t and becomes prominent causing hump-type leakage. Negative V_{gb} suppresses this n-channel leakage current completely. If special implantation technologies are used to intentionally increase the edge doping concentration and stress at the Si island edge is decreased, hump-type leakage can be prevented. In PMOS devices, type E leakage is rare since phosphorus diffusion to nearby oxides is unlikely. Another possibility is the well-known corner effect of mesa isolated devices.[9,10] In this case a large angle tilt field implant aiming for the corners or lateral isolation is known to solve the problem.[10]

Leakage mechanism models of NMOS devices are proposed and divided into five types, most of which are unique to SOI devices. However, PMOS devices showed only types A, B, and E. By first identifying leakage characteristics in the Fig. 1 like plots and later by $I_d - V_g$ measurements, mechanisms of device leakage can be identified. Both high defect density and high stress, which affects dopant diffusion, are very critical in type D leakage and should be minimized.

The authors thank Ed Hall, Peter Gill, and Fabio Pintchovski for supporting this study.

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