Degradation of ultrathin oxides by iron contamination

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Iron-contaminated oxides of metal-oxide-semiconductor devices were investigated to study gate oxide integrity (GOI) degradation dependence on oxide thickness for oxide thicknesses from 3 to 5 nm and iron densities from 4×10^{10} to $1.4\times10^{12}\,\mathrm{cm}^{-3}$. In contrast to other publications, we show that oxides as thin as 3 nm show gate oxide integrity degradation, especially for the higher iron densities. But even for the low iron density we observe GOI degradation for all oxides. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1410363]

Gate oxide integrity (GOI), the ability of a metal-oxide-semiconductor (MOS) device to remain operational for many years with a gate voltage applied, is one of the most important device parameters in integrated circuits. Oxide electric fields during device operation are typically significantly below the oxide breakdown electric fields. For example, nominal oxide electric fields are around $5-6\times10^6$ V/cm ($V_G \approx 5$ V for 10 nm oxides and $V_G \approx 2.5$ V for 4 nm oxides) while the breakdown oxide electric field is around $10-15\times10^6$ V/cm. Actual electric fields may be higher if the semiconductor surface is not planar. For example, surface roughness, crystal originated pits (COPs), and metallic precipitates create locally high electric fields due to their nonplanar nature coupled with possible local oxide thinning. The issue of surface roughness has not yet been definitively resolved. Some work suggests that surface roughness impairs oxide integrity while others feel that surface roughness has little effect. When COPs are at or near the surface, they degrade GOI, but this effect diminishes for thinner oxides.[1]

Much work has been done on the effect of metallic impurities on GOI, because possible metal contamination is an ever-present issue during integrated circuit manufacturing. It is generally acknowledged that metals degrade thick oxides, i.e., oxides 10 nm thick or thicker. The effect of metals on thin oxides is not so clear, partly because less work has been reported on ultrathin oxides. For example, a detailed study of the effects of Cu and Ni contamination on 5–17 nm oxides showed that thicker oxides ($t_{ox} \geqslant 7.5$ nm) were more seriously degraded than thinner oxides ($t_{ox} < 7.5$ nm).[1] Cu contamination had a higher impact on GOI than Ni. GOI was also influenced by the type of substrate, i.e., whether the substrates were bulk Si wafers, p/p^+, or p/p^{++} epitaxial wafers. This substrate effect is related to the gettering ability of the substrates. Cu-contaminated ultrathin oxides ($t_{ox} = 3$ nm) showed enhanced oxide leakage currents, lower oxide breakdown electric field, and lower charge to breakdown for Cu contamination as low as 10 ppb compared to uncontaminated samples.[2] So, we have the dilemma of both reduced and unchanged GOI as contaminated oxides become thinner. We have investigated the effect of Fe contamination on the GOI of oxides 3–5 nm thick. Iron is one of the most technologically important impurities in silicon.[3] Recent reviews detail many of the effects of Fe in Si and provide numerous references to previous publications.[4,5] The International Technology Roadmap for Semiconductors calls for iron densities below $10^{10}\,\mathrm{cm}^{-3}$ for future Si processing.[6]

We used (100) oriented, boron-doped, 10-μm-thick, p-type epitaxial layers (30 Ω cm resistivity) on p^+ substrates. Iron was introduced by dipping the wafer into a solution of 10 ppb in SC1 for 30 min, resulting in a surface iron density of $10^{13}\,\mathrm{cm}^{-2}$. The wafers were subsequently heated at 900, 950, and 1000 °C for 2 h resulting in volume iron densities of 4×10^{10}, 5×10^{11}, and $1.4\times10^{12}\,\mathrm{cm}^{-3}$. The iron density was determined by deep level transient spectroscopy (DLTS) measurements on the front wafer surface after iron drive in. Schottky diodes were fabricated by aluminum-evaporated contacts on the front surface and a large-area silver paste contact on the back surface. The oxides were grown at 900 °C in a rapid thermal annealing system for various times. The oxide thickness was measured ellipsometrically giving the thicknesses: 3.04, 3.07, 3.06, 3.06 nm for the reference, the 4×10^{10}, the 5×10^{11}, and the $1.4\times10^{12}\,\mathrm{cm}^{-3}$ contaminated samples, respectively. For the other wafers the relevant thicknesses were: 4.03, 4.01, 4.06, and 4.01; and 4.91, 5.05, 5.08, and 5.03 nm. The gates consisted of 200 nm, n^+ poly-Si, doped with phosphorus to a sheet resistance of 25 Ω/square.

We used two types of GOI measurements. The first is the well-known ''time-zero'' measurement in which a negative gate voltage is swept over the voltage range from zero until the current reaches some preset value and the resulting gate current is measured. In the second, we used the ramped gate current technique. Here the gate current is ramped from 10^{-11} to 10^{-1} A or less, depending on the oxide breakdown, and the resulting gate voltage is measured. We illustrate this technique in Fig. 1, where we show the 4 nm oxide V_G-I_G characteristics. The early part of the curves is determined by $I = C dV_G/dt$ and after the first discontinuity it is determined by Fowler–Nordheim tunneling for the thicker oxides and by direct tunneling for the thinner oxides. We choose the first sharp discontinuity as the oxide breakdown criterion. We find this technique to work well for all oxides we have investigated whether contaminated or uncontaminated. The breakdown characteristics are not always unambiguous for the

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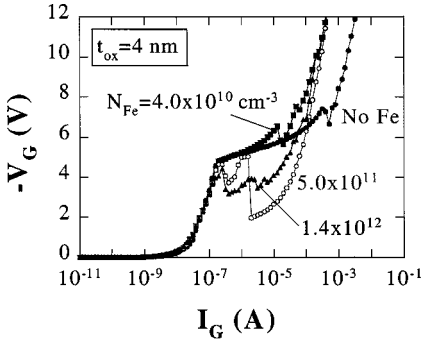

FIG. 1. Voltage–current characteristics for the ramped gate current technique for the 4 nm oxides.

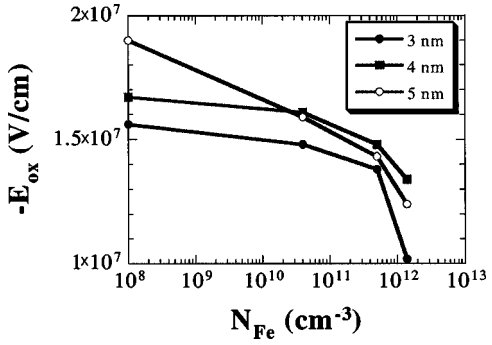

FIG. 3. Breakdown oxide electric field vs iron density as a function of oxide thickness.

time-zero I_G-V_G measurements. The thin, contaminated oxides often do not exhibit a clear breakdown characteristic.

We show the key results in Fig. 2 as Weibull plots. Since the devices were measured with both gate and substrate in accumulation, we determined the oxide electric field simply by dividing the oxide breakdown voltage by the oxide thickness, neglecting the small voltage drops across the accumulated substrate and gate. The sum of these drops is around 0.4 V in our case and considering it would reduce the electric field by $0.8-1.3\times10^6$ V/cm. These figures clearly show the degrading effect of the iron contamination. For all oxide thicknesses we note the oxide breakdown electric field to degrade with increased contamination. Although the 5 nm curves exhibit the highest dispersion, there is still a significant dispersion even for the 3 nm oxides. A plot of the 50% failure points as a function of oxide thickness and iron density is shown in Fig. 3. The "$N_{Fe}=10^8$ cm^{-3}" points correspond to no intentional iron contamination. The 5 nm data show the highest negative slope over the entire N_{Fe} range, as expected. The other two exhibit a relatively modest slope for the lower iron densities, but for the highest iron density, all three curves drop steeply.

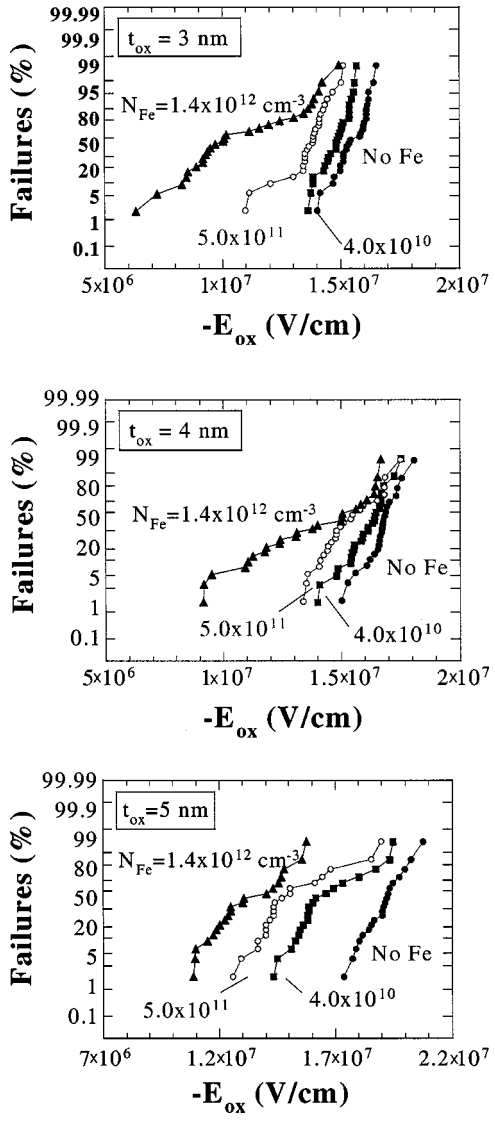

FIG. 2. Weibull plots of breakdown oxide electric field for the three oxide thicknesses.

Although we cannot make minority carrier lifetime or diffusion length measurements, due to the epitaxial layer, we have made frequency-dependent conductance and capacitance measurements of the MOS capacitors, fabricated on thicker oxides on the same wafers. Such information can be used to extract lifetime information of the gate-induced space-charge region, i.e., the first micron or so from the SiO_2–Si interface.[7] The results from these reduced near-surface lifetimes agree with the degraded GOI data, i.e., the worst GOI degradation corresponds to the lowest lifetime.

The deleterious effect of iron on oxide integrity is well known. Istratov, Hieslmair, and Weber recently published data of the effect of iron density on oxide breakdown and showed that as oxide thicknesses are reduced, the critical iron density for oxide breakdown also decreases.[5] A least square fit to published data yielded the relationship between critical iron density, N_{crit} (in cm^{-3}) and oxide thickness t_{ox} (in nm)

$$N_{crit}=1.53\times10^{11}\,10^{0.12t_{ox}}.$$

Their data extend from 30 to 5 nm oxide thicknesses for which the critical iron density is 6×10^{11} cm^{-3}. We find that $N_{Fe}=4\times10^{10}$ cm^{-3} still influences the 5 nm oxide breakdown (Fig. 3). That same iron density, however, has much less influence on oxide breakdown of 3 and 4 nm thick oxides.

The cause of gate oxide integrity degradation has been attributed to Fe precipitate formation at the SiO_2/Si interface, which can penetrate into the oxide.[8] This can lead to local oxide thinning, enhanced electric field at sharp points of a precipitate,[9] formation of iron-related traps in the

oxide,[10] decomposition of the oxide in the presence of the metal,[11] and even the formation of metal silicates in the oxide.[12]

In summary, gate oxide integrity measurements of iron-contaminated MOS devices showed degradation for 3- , 4- , and 5-nm-thick SiO_2 for iron densities of 4×10^{10}, 5×10^{11}, and $1.4\times10^{12}\,cm^{-3}$. Although the 5 nm oxide degraded the most, the thinner oxides still exhibited some degradation, even for the 3 nm oxide.

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