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Characterization of Strained Si/SiGe with Raman, Pulsed MOS Capacitor and Gate Oxide Integrity Measurements

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We use several characterization techniques including Raman spectroscopy, pulsed metal-oxide-semiconductor (MOS) capacitor capacitance-time, and gate oxide integrity measurements to characterize strained silicon/relaxed SiGe/graded SiGe/Si samples. The effective generation lifetime depends on the defect density in the various layers varying from 10^{-4} s near the surface to 10^{-7} s in the graded and highly defective SiGe. GOI statistical analysis shows worsening oxide breakdown as the Ge concentration in the SiGe increases.

Introduction

Strain-induced mobility variation in silicon has been known for years and had been considered a problem rather than an advantage (1-3). In recent years, strained silicon has generated significant interest in the Si integrated circuit community because the manipulation of strain has created an opportunity for carrier mobility enhancement. Different approaches of introducing strain are being studied. One of the approaches for introducing strain in the Si channel region is the strained Si/SiGe heterostructure, consisting of a thin strained Si layer grown on a relaxed SiGe grown on a graded SiGe layer on top of a standard Si substrate.

We use Raman spectroscopy, pulsed MOS capacitor *C-t* and GOI measurements to characterize the strained silicon/relaxed SiGe samples and the gate oxide grown on the strained Si. Raman spectroscopy was used to evaluate the strain in the Si layer. MOS capacitors were fabricated on the strained Si samples and also on Si control samples for pulsed MOS capacitor *C-t* and GOI measurements to determine the generation lifetime and characterize the gate oxide quality.

Experiments and Sample Preparation

Raman Spectroscopy – Strain Evaluation

All of our strained Si samples have strained Si layers close to or exceeding the theoretical critical thickness (h_c). It is important to verify the strain/relaxation status of the strained Si samples before electrical measurements. Raman spectroscopy is an optical characterization technique that provides information of material composition and strain. The incident light is scattered from the surface of the sample. Part of the scattered light wavelength is shifted due to the interaction of the incident light with optical phonons and the transfer of energy to the lattice vibrations in the optical branch (4). For bulk Si with its optical phonon vibration frequency of 15.6×10^{12} Hz, the Raman shift is about 520 cm^{-1}. For strained Si or strained SiGe, the change of lattice constant causes a change of

vibration frequency and the Raman shift deviates from that of bulk Si or bulk SiGe. By calculating the deviation of the Raman shift, we are able to extract the in-plane strain. The incident light wavelength in this study is 364 nm. For Si, the absorption coefficient is about 8.4×10^{5} cm^{-1} giving a sampling depth (1/2 of the penetration depth) of about 6 nm (5, 6).

Pulsed MOS Capacitor

Due to the presence of misfit dislocations and threading dislocations in the strained Si/SiGe structure, the carrier lifetime is suitable to characterize such defects. The pulsed MOS capacitor technique is used to determine the carrier generation lifetime τ_g. A pulsed gate voltage is applied to the MOS capacitor under test and drives the capacitor from accumulation into deep depletion. The transient capacitance is measured with respect to time from deep depletion to inversion. The effective generation lifetime is extrapolated from the slope of the *Zerbst plot*, $-d(C_{ox}/C)^2/dt$ versus $(C_{inv}/C - 1)$ according to the following equation (6)

$$-\frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2 = \frac{2n_i}{\tau_{g,eff} N_A}\frac{C_{ox}}{C_{inv}}\left(\frac{C_{inv}}{C} - 1\right) + \frac{2K_{ox} n_i s_{eff}}{K_s t_{ox} N_A} \qquad [1]$$

The effective generation lifetime is a measure of the depletion region generation lifetime τ_g and surface generation velocity s_g (6). For the measured strained Si samples, it is expected that the defects in both strained Si and SiGe layer are dominant over the defects at the surface leading to the approximation of effective generation lifetime $\tau_{g,eff} \approx \tau_g$. τ_g is sometimes written as (7)

$$\tau_g \approx \tau_r e^{|E_T - E_i|/kT} \qquad [2]$$

where τ_r is the Shockley–Read–Hall (SRH) recombination lifetime and E_T is the trap energy level. τ_r can be expressed as

$$\tau_r = \frac{1}{\sigma v_{th} N_T} \qquad [3]$$

where σ is the carrier capture cross section, v_{th} the carrier thermal velocity, and N_T the trap density. If we make the assumptions that the defects of the strained Si and SiGe are deep-level traps and located at about the middle of the band gap ($E_T \approx E_i$), the carrier capture cross section is about 10^{-15} cm^2, and the carrier thermal velocity is 10^7 cm/s, we are able to obtain approximate defect density N_T from the generation lifetime (8).

Since the strained Si samples are undoped in both strained Si and SiGe layers and the SiGe layer is much thicker than the strained Si layer, the depletion region edge during *C-t* measurement extends into the SiGe layer. The intrinsic carrier concentration n_i used for extracting τ_g is (9)

$$n_{i,\mathrm{SiGe}} = n_{i,\mathrm{Si}} \exp\left(\frac{E_{G,\mathrm{Si}} - E_{G,\mathrm{SiGe}}}{2kT}\right) \qquad [4]$$

where $n_{i,\mathrm{Si}}$ is the intrinsic carrier concentration of Si, $E_{G,\mathrm{Si}}$ and $E_{G,\mathrm{SiGe}}$ are the band gaps for Si and SiGe, respectively.

Gate Oxide Integrity

Since higher interface trapped charge density was found in previous *C-V* measurements for the strained than for the unstrained SiO_2/Si interface, it raises a concern regarding gate oxide integrity. To study the gate oxide quality, we made GOI measurements in the form of "time zero breakdown" (TZBD) measurements, where the gate voltage is ramped and the gate current is measured and plotted as $\log I_G - V_G$. The oxide breakdown voltage is sensitive to the gate voltage ramp rate. Low ramp rates allow more time for oxide defect creation, leading to lower breakdown voltage (6). We used a ramp rate of 1 V/s.

Sample Preparation

The strained Si samples are (100) p-type silicon substrates with a graded SiGe layer (Ge fraction from 0% to x% at a gradient of 10% Ge/μm) deposited on top and followed by a relaxed SiGe layer with constant Ge fraction (x%). Some of the samples have a strained Si overlayer. The substrates are p^+, doped with boron to 10^{19} cm^{-3}. There is no intentional doping in the SiGe or Si layers. These samples come with different Ge fractions in the SiGe buried layer forming different amounts of strain in the strained-Si film, if there is a Si film on top. Because of the thick SiGe buffered layers, they are strain-relaxed and all cap Si films are biaxially tensile strained. Table I lists the samples in this study.

TABLE I. SiGe Samples.

Sample No.	Ge Fraction x	Graded Ge	Constant Ge	Strained-Si
70219V	15%	1.5 μm	1.2 μm	0.04 μm
70219S	15%	1.5 μm	1.2 μm	0.08 μm
70226B	15%	1.5 μm	1.2 μm	0.14 μm
70226A	20%	2.0 μm	1.2 μm	0.14 μm
50568H	26%	2.6 μm	2.0 μm	0.04 μm
50565J	32%	3.2 μm	2.0 μm	0.06 μm
70221N	42%	4.2 μm	1.2 μm	0.05 μm

Samples were prepared for different measurements. Raman measurements, being contactless and non-destructive technique, required no prior treatment for the measurement and the raw samples were used directly. For pulsed MOS capacitor and GOI measurements, MOS capacitors were fabricated on five strained Si samples and a *p*-type Si control wafer. In order to avoid strain relaxation and dislocation propagation from the buffer layers, high temperature processing (>700°C) is undesirable (10). Several publications have used conventional oxide processing at 700 to 850°C for strained Si MOSFET fabrication (10-12). We used a 2-hour dry oxidation, 2-hour wet oxidation, and 2-hour dry oxidation at 750°C. The oxide thickness is about 15 nm. After oxidation, 500 μm diameter Al gates were evaporated, followed by a 450°C anneal in a forming gas ambient for 20 minutes to reduce oxide interface defects. Each sample has at least 150 MOS devices formed on it. Table II lists all samples made for the different measurements.

TABLE II. Samples Prepared for Measurements.

Sample No.	% Ge	Strained-Si	Raman	Pulsed MOS Capacitor/GOI
Si-Control	-	-	√	√
70219V	15%	0.04 μm		√
70219S	15%	0.08 μm	√	
70226B	15%	0.14 μm	√	√
70226A	20%	0.14 μm	√	√
50568H	26%	0.04 μm	√	
50565J	32%	0.06 μm	√	√
70221N	42%	0.05 μm	√	√

Experimental Results and Discussion

Raman Spectroscopy – Strain Evaluation

Figure 1 shows UV-Raman data of strained Si grown on relaxed SiGe buffers using the Ar-Ion 364nm line. The redshift in the Si-Si LO phonon frequency from unstrained bulk Si (black curve) indicates the presence of tensile strain. Using the appropriate Si-Si phonon deformation potential, one can calculate the strain magnitude from the shift in frequency. Table III summarizes the corresponding frequency shifts, %Ge from HRXRD measurements, in-plane biaxial strain, and the percent of maximum achievable strain in the Si cap. Although a few of the higher Ge concentration samples may have exceeded the theoretical critical thickness for the strained Si cap, the Raman data suggest the Si layers are fully strained and in some cases, may have exceeded 100% of the maximum strain. This could be due in part to errors associated with measuring the phonon deformation potential and the difference in thermal expansion coefficients between the Si and SiGe layers.

The phonon peak widths or phonon lifetimes can also provide a qualitative assessment of the film crystallinity. In this case, the peak widths are within a few percent of unstrained bulk Si, indicating relatively few defects.

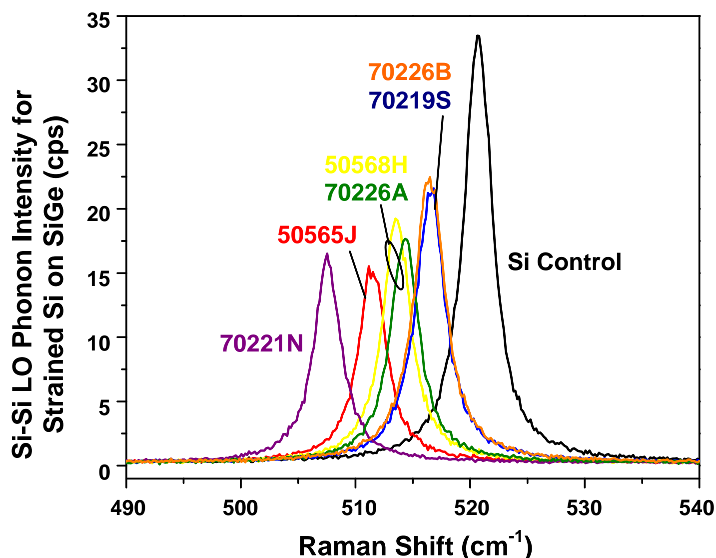

Figure 1. Raman spectra of the Si-Si LO phonon in strained Si on SiGe using UV excitation at 364nm.

TABLE III. Strain extraction for strained Si on SiGe virtual substrates from Raman shift.

Sample	%Ge	Exp. (cm^{-1})	Δ from relaxed Si (cm^{-1})	Strain $\varepsilon_{\|}$	Raman shift for fully Strained Si (cm^{-1})	% Strained	Measured FWHM (cm^{-1})
Si-Contl	-	520.70	-	-	-	-	2.97
70219S	14.7	516.56	-4.14	0.0056	516.60	101.0	3.11
70226B	14.8	516.48	-4.22	0.0057	516.57	102.2	3.22
70226A	20.0	514.30	-6.40	0.0086	515.08	113.9	2.98
50568H	27.3	513.59	-7.11	0.0096	512.95	91.9	2.94
50565J	33.4	511.47	-9.23	0.0124	511.15	96.6	2.94
70221N	42.2	507.55	-13.15	0.0177	508.50	107.8	2.87

We have also used high resolution X-ray diffraction (HRXRD) reciprocal mapping to confirm the Raman strain results. Figure 2 shows an asymmetric (224) reflection from sample 50565J, expressed in a direct space representation. Distinct peaks are observed for the Si substrate (red), the constant SiGe buffer (orange), and the Si cap layer (blue). For the graded SiGe layer (green), a continuum of lattice constants is found spanning the range bound by the substrate and the constant buffer. Since an asymmetric reflection has components of the scattering vector parallel to the in- and out-of-plane lattice constants, it provides a direct measurement of both parameters. As was found for all strained Si samples investigated in this work, the reflection for the strained Si cap lies at the same in-plane lattice constant as the constant SiGe buffer, indicating a coherently grown Si layer. In this case, XRD results found an in-plane lattice constant of 5.50 Å for the Si cap and SiGe buffer which corresponds to a biaxial Si strain of +1.27%, very close to the Raman strain value of +1.24%.

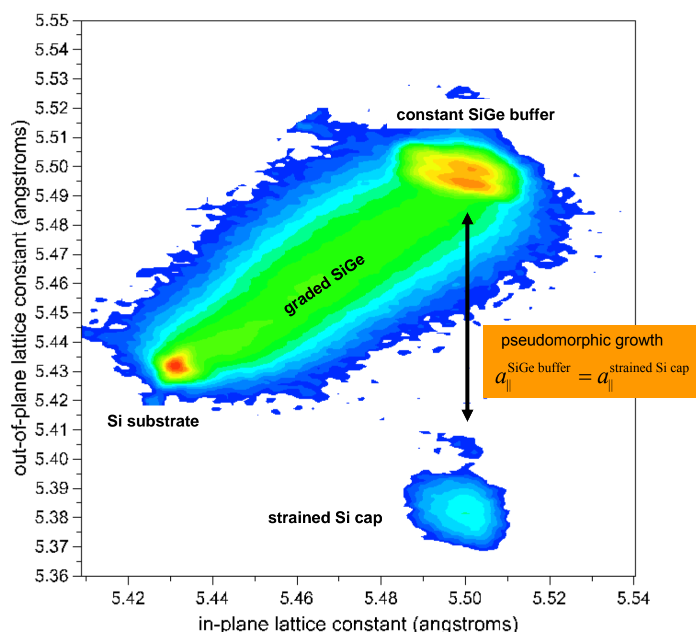

Figure 2 HRXRD reciprocal mapping for sample 50565J.

<u>Pulsed MOS Capacitor</u>

For pulsed MOS capacitor measurements the gate voltage was pulsed from V_{Gi} = -4 V to V_{Gf} = 3 V. The *C-t* curves for the tested samples are plotted in figures 3(a) for the Si control sample and (b) for the SiGe samples, clearly showing that the Si control sample has the longest relaxation time while for the SiGe samples, higher Ge fraction leads to

shorter relaxation times. In addition, for samples with the same Ge fractions (samples 70219V and 70226B, 15%), the thicker strained Si layer gives a shorter relaxation time probably due to higher dislocation density in the thicker strained Si layer.

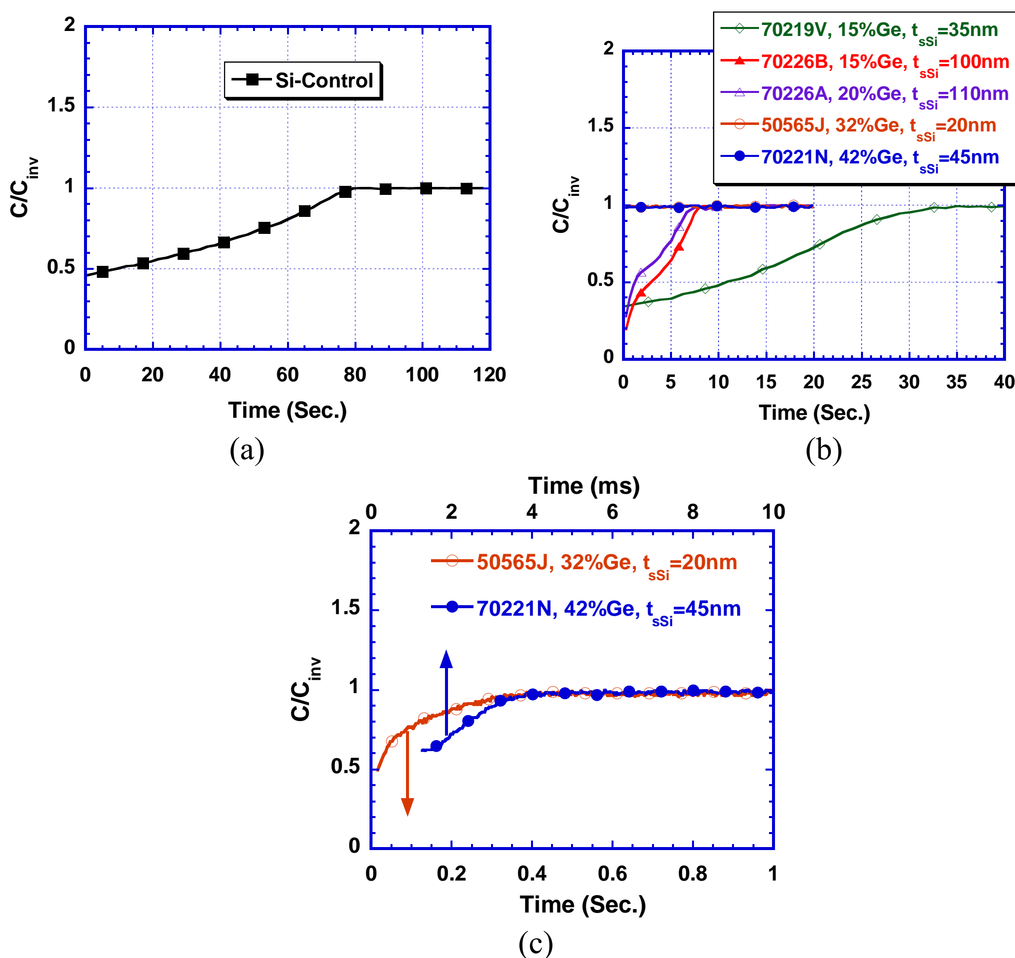

Figure 3. *C-t* curves for (a) Si control, (b) SiGe samples, and (c) higher strain samples.

For the higher strain samples (samples 50565J, 32% Ge and 70221N, 42%), the relaxation time is very short. Figure 3(c) shows the *C-t* curves for these two samples. The strained Si thicknesses shown in the plots are extracted from previously made *C-V* measurements. These extracted values of all measured samples are somewhat lower than those provided by the sample supplier listed in table I. This is due to a number of oxidation, oxide etch, and cleaning process performed prior to MOS capacitor fabrication which results in strained Si consumption.

The effective generation lifetime is plotted in figure 4. It confirms the same trends of *C-t* curves: higher Ge composition and thicker strained Si layer lead to poorer generation lifetime. The approximate defect density N_T is also calculated and plotted in the figure according to equations [4] and [5] by assuming the trap energy level E_T to be E_i, the carrier capture cross section σ to be 10^{-15} cm^2 and the carrier thermal velocity v_{th} to be 10^7 cm/s. A high-quality Si wafer contains defect densities on the order of 10^{10} cm^{-3} (8). Our measurements indicate the defect density for the Si-control is about 10^{12} cm^{-3}, which is moderate. However, for the strained Si samples, the defect densities range from 10^{13} to 10^{16} cm^{-3}, indicating degradation in strained Si and SiGe layers. We determined these

densities based on the assumptions $E_T = E_i$ and $\sigma = 10^{-15}$ cm^2, neither of which is known. For line defects, *e.g.*, dislocations, the lifetime expression is likely to be quite different and hence the defect densities of figure 4 are only first order values of equivalent point defect densities.

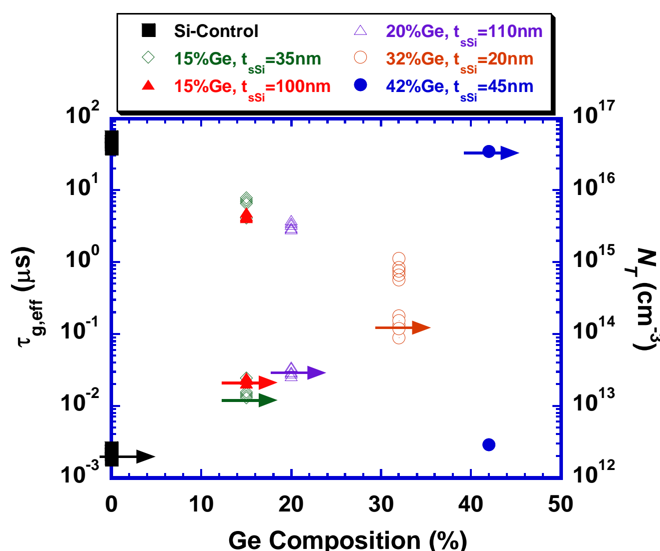

Figure 4. Effective generation lifetime and defect density for Si control and different SiGe samples.

Since some *C-t* curves in figures 3 show a rapid transient at the beginning after the pulse is applied, we chose one of the samples 70226B and measured it with different pulsed voltages for a closer observation. Increasing gate voltages drive the depletion region deeper into the sample. Figure 5(a) shows the *C-t* plot for the gate voltage pulsed from V_{Gi} = -4 V to V_{Gf} = 0, 0.5, 1.5, 2, 3, and 4 V. Only curves with pulsed voltages higher than 2 V show a rapid transient. From the measured capacitance we calculated the depletion region width. It is found that the rapidly changing transients occur when the depletion region enters the graded SiGe layer. As the depletion region collapses with time, its time dependence changes as it leaves the highly defective region. The curves in figure 4 show that this occurs when the depletion region leaves the graded SiGe layer which has a higher defect density than the relaxed SiGe layer. The Zerbst plot is given in figure 5(b) for the *C-t* curve with final pulsed voltage 4 V, clearly showing two linear sections. The effective generation lifetimes from these two sections are 1.6 µs and 0.07 µs for the depletion regions before and after entering the graded SiGe layer, indicating that more defects in the graded SiGe layer dramatically reduce the generation lifetime. A high defect density in the graded SiGe layer may be due to a high dislocation density, confirmed by published TEM measurement shown in figure 6 (13). The dislocations in the graded SiGe layer are mainly *misfit dislocations* (MDs) which can be replicated into the epitaxial film during the layer growth and form *threading dislocations* (TDs) (14). Threading dislocations originating from the graded SiGe layer, and propagating through the strained Si layer, are known to increase with Ge fraction.

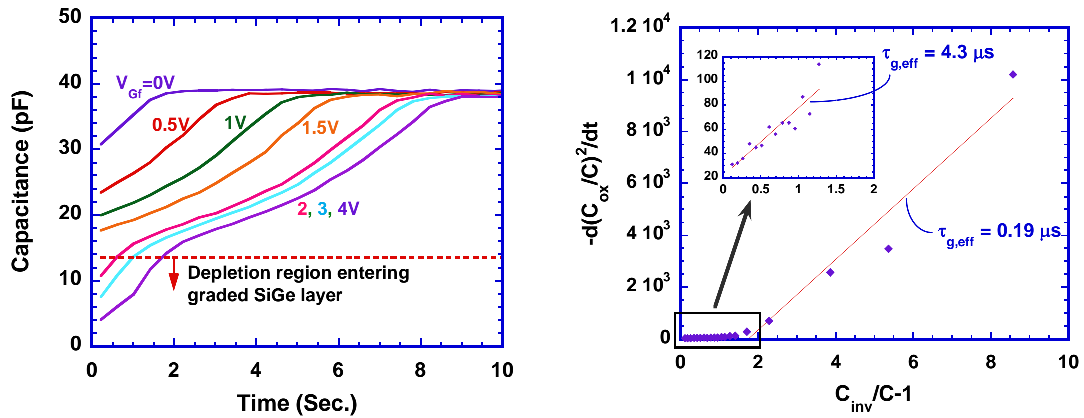

Figure 5. (a) *C-t* curves for sample 70226B with different pulsed voltages and (b) Zerbst plot.

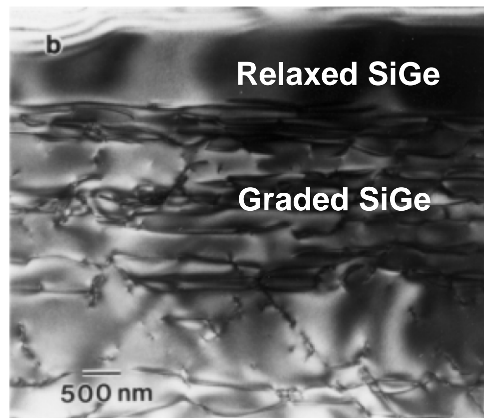

Figure 6. TEM micrograph for a relaxed SiGe/graded SiGe structure (13).

Gate Oxide Integrity

Due to possible misfit dislocations in the relaxed SiGe virtual substrate propagating into the strained Si overlayer or partial strain relaxation in the strained Si layer generating dislocations, the surface of strained Si is likely poorer than a regular Si substrate. Interface trapped charge density may increase and degrade the oxide integrity. Therefore, time-zero breakdown (TZBD) GOI measurements were made on 120 MOS devices on each tested sample. Figure 7 show the TZBD data. Each plot contains eight randomly selected TZBD curves from 120 measurements. While the Si-control sample shows typical breakdown characteristics, all other strained Si samples exhibit irregular behavior with either lower breakdown voltages or broadened breakdown distribution.

Some of the devices break down briefly at low voltages and then recover and switch to normal *I-V* curves and break down again. A possible reason is that some defects start to break down with increasing current density. If the localized breakdown region is sufficiently small, it is possible for the localized region to “heal” itself and the device returns to a “normal” device. This is sometimes referred to as an *electrical* breakdown. The device then breaks down finally at a higher voltage, likely due to a combination of electrical and thermal breakdown. In addition, sample 70221N (highest strain film with 42% Ge) clearly has lower breakdown voltages indicating poor oxide quality.

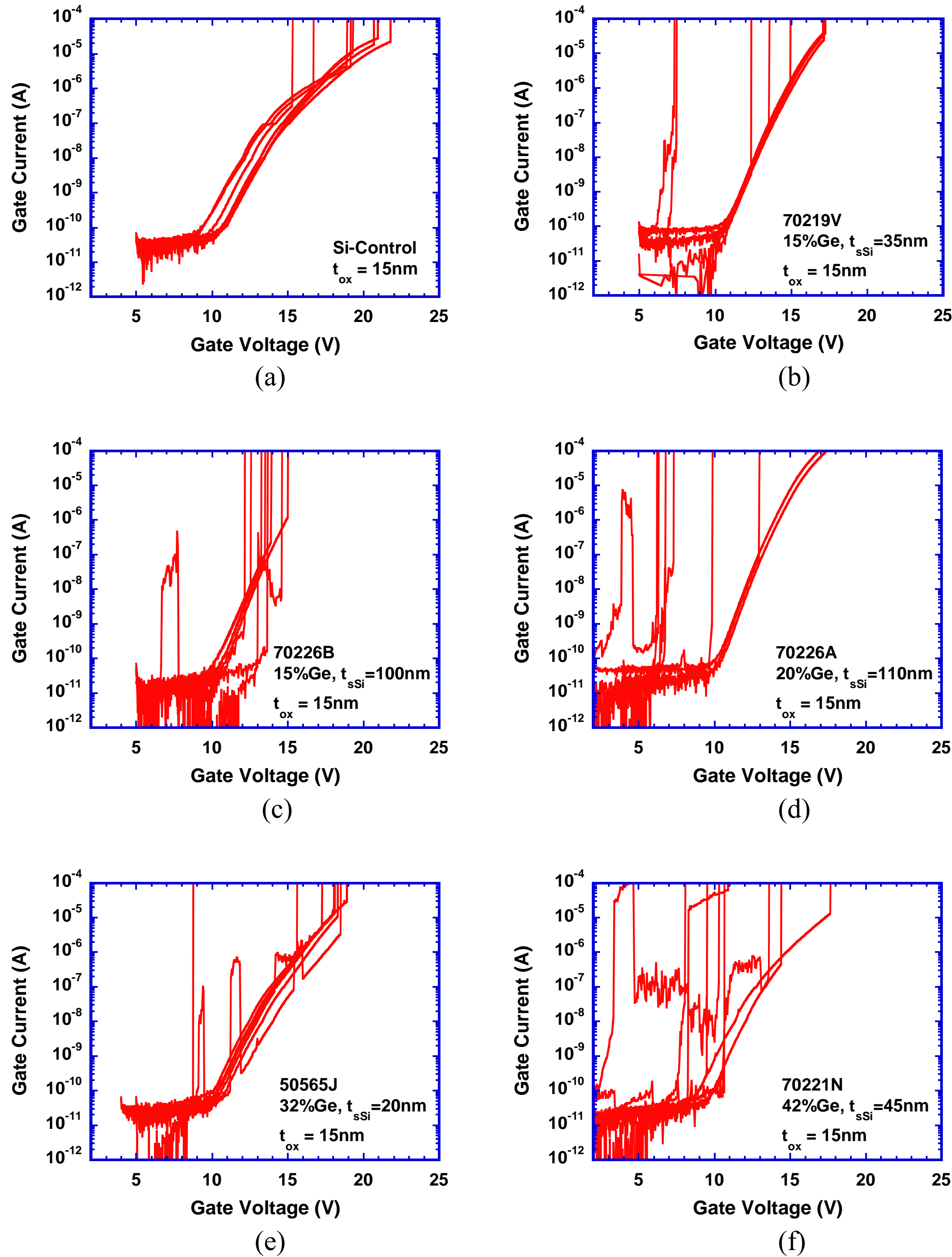

Figure 7. Time-zero breakdown gate oxide integrity measurement for samples (a) Si-control, (b) 70219V, (c) 70226B, (d) 70226A, (e) 50565J, and (f) 70221N.

The number of failures as a function of oxide breakdown voltage is given in figure 8. While the Si-control sample shows typical *intrinsic breakdown* characteristics, most of the strained Si samples exhibit a twin-peak distribution, where the first peak at the lower breakdown voltages is *defect-related breakdown* and the second peak at the higher voltages is *intrinsic breakdown*. For the highest strained sample (70221N, 42% Ge), the defect-related breakdown is dominant and the intrinsic breakdown is not observed. Although the trend that higher strain leads to worse GOI indicating poorer oxide quality

is seen, there is an exception. The second highest strain sample (50565J, 32% Ge) exhibits the best GOI characteristics over all strained Si samples. The reason is not clear at the moment. We are currently conducting more experiments to examine this phenomenon. Moreover, although not shown here, we also find higher interface trap densities at the oxide/Si film interface for the strained samples compared to bulk Si wafers.

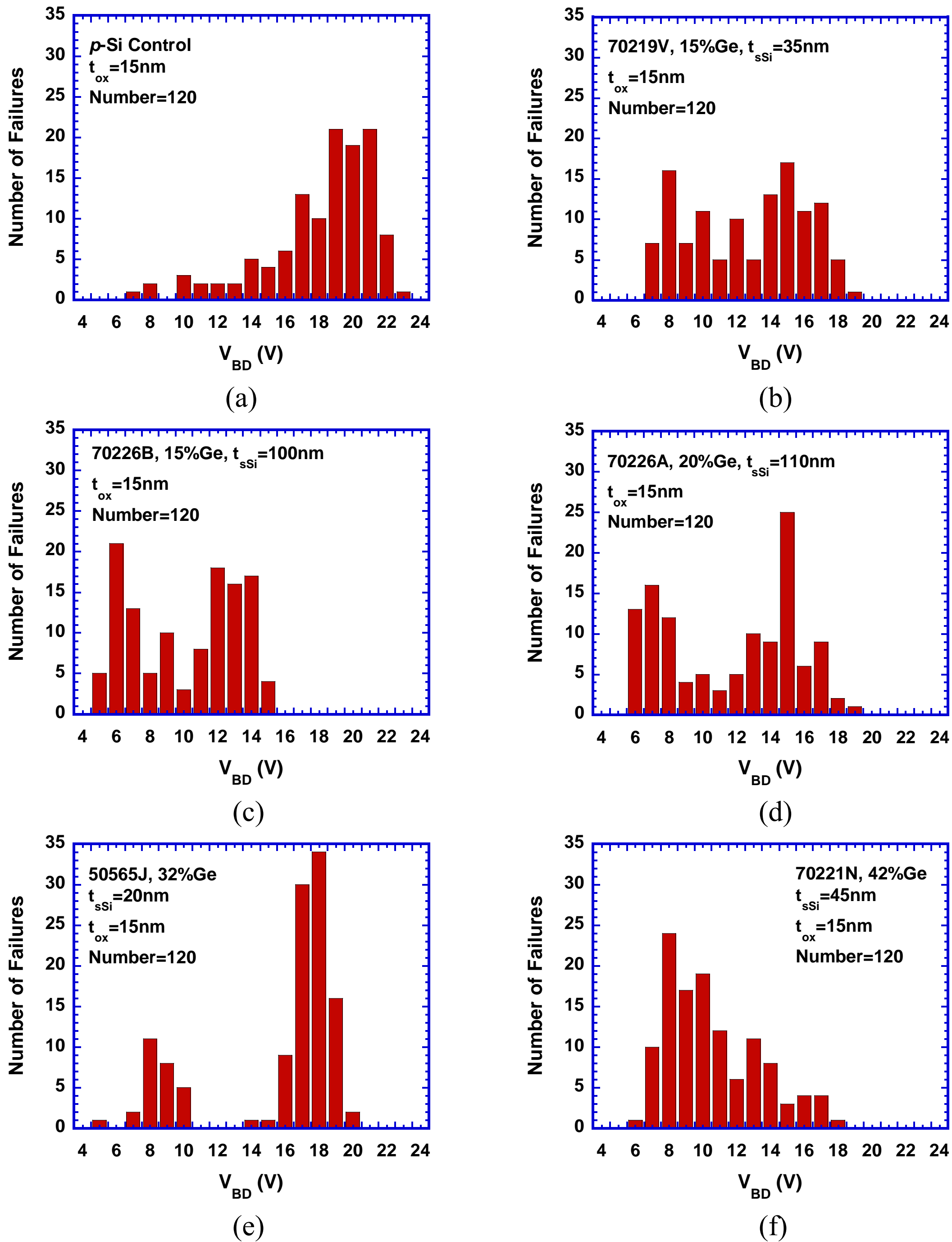

Figure 8. Number of failures versus oxide breakdown voltage.

Figure 9 is the cumulative failure distribution plot. Again, the defect-related breakdown behavior is clearly observed for all strained Si samples with significantly reduced breakdown voltages.

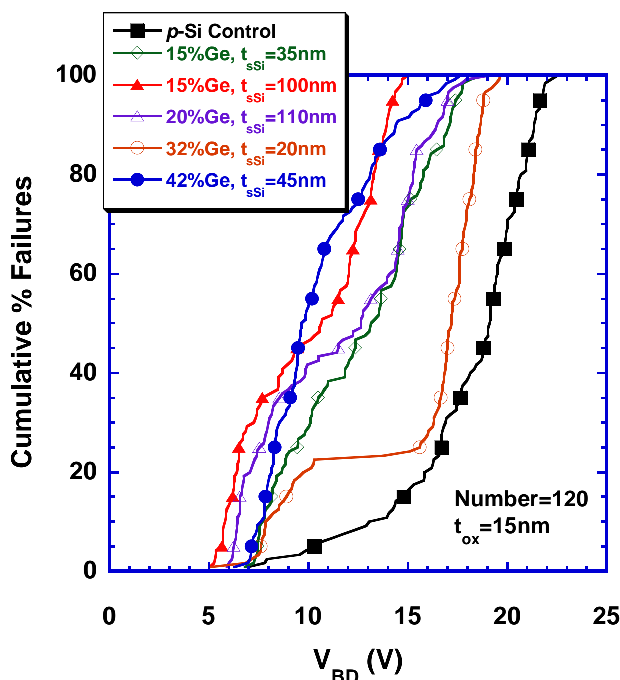

Figure 9. Cumulative percent failure versus breakdown voltage.

Conclusions

We have used Raman spectroscopy, pulsed MOS capacitor, and GOI measurements to characterize the strained Si of Si/SiGe/Si samples. Raman spectroscopy measures the strain in the strained Si layer. We found that although the strained Si layers of all samples are either close to or exceed the theoretical critical thickness, they are still fully strained. The effective generation lifetime of strained Si samples is obtained by Zerbst analysis of pulsed MOS capacitor measurement. It is found that higher strain and thicker strained Si layers cause shorter generation lifetime. It is also found that the generation lifetime is very short in the graded SiGe layer due to higher defect densities in the graded SiGe. Lifetime measurement results inspired us to examine the gate oxide quality of strained Si layers. The GOI measurement was performed to provide a statistical analysis of the gate oxide quality. All strained Si samples show clear defect-related breakdown behavior while the Si control sample shows mainly intrinsic breakdown characteristic. Since the depletion region width extends into the strained Si and relaxed SiGe layers during *C-t* measurements, the measured effective generation lifetime is affected by strained Si/SiO_2 interface states and defects in the strained Si and SiGe layers. On the other hand, the GOI measurements are affected by Si/SiO_2 interface states and dislocations and other defects that reach the strained Si surface or penetrate into the oxide. In this sense, pulsed MOS capacitor and GOI measurements complement each other.

Acknowledgments

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