Effect of Surface Preparation on the Current–Voltage Behavior of Mercury-Probe Pseudo MOSFETs

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***Abstract*—Surface preparation has a significant effect on the drain current–gate voltage characteristics of mercury-probe pseudo MOSFETs. Surface preparation by dilute hydrofluoric acid (HF) rinse manifests itself in two ways: it changes the barrier height of the Hg/Si Schottky barrier and it induces charge on the Si-film surface. Consequently, the electron drain current decreases with time after the HF rinse and the hole current increases. The surface charge also influences the extraction of the interface-trap density at the Si/buried oxide interface.**

***Index Terms*—Interface trap density, pseudo MOSFET, Schottky barrier, semiconductor device measurements, silicon, silicon-on-insulator, surface charge, threshold voltage.**

I. Introduction

THE PSEUDO MOSFET (Ψ MOSFET) is a simple, yet powerful, device to characterize various aspects of silicon-on-insulator (SOI) wafers [1], [2] and is routinely used for incoming wafer inspection to determine material parameters [3]–[7]. It comes in the point contact and the mercury-probe configurations. The mercury-probe pseudo MOSFET (HgFET) is similar to Schottky source/drain MOSFETs [8]. The major differences are that in the HgFET, the gate overlaps the source and drain, but the HgFET channel is on the side of the Si film opposite to the source/drain side. The point-contact Ψ MOSFET is easy to implement, simply requiring two probes on an SOI wafer. However, the contact geometry is poorly defined leading to questions in the interpretation of the $I_D - V_G$ data. Initially, the conventional MOSFET drain current equation was used with a correction factor of 0.75 to account for the point-contact geometry [1]. More recently, a detailed study of the drain current showed the correction factor to depend on probe pressure, silicon island size, and probe spacing [9]. The HgFET has the advantage of well-defined source/drain contacts, but it has an Hg/Si interface and all the vagaries that accompany metal/Si contacts, where barrier heights change with time due to surface state changes. The Si surface must be properly treated to characterize HgFETs. One of the advantages of Ψ MOSFETs is that both electron and hole conduction can be characterized by using appropriate gate voltages. Similar to Schottky drain/source MOSFETs, the Schottky barrier height for the channel carriers (electrons for n-channel and holes for p-channel MOSFETs) must be low. In an HgFET, low-barrier heights for holes and electrons must be realized. Since the barrier height cannot be simultaneously low for electrons (ϕ_{Bn}) and holes (ϕ_{Bp}), one must find a way of having a low-electron barrier height at some time and a low-barrier height for holes at another time. It is commonly done by rinsing the SOI surface in dilute HF. This ensures a low-electron barrier height immediately after the HF rinse. With time, the surface condition changes, the electron barrier height increases while the hole barrier height decreases.

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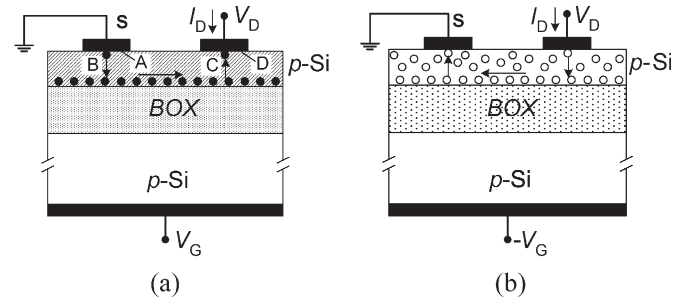

Fig. 1. HgFET cross sections showing (a) electron and (b) hole path impediments. The space-charge regions under the Hg contacts in (b) are not shown for simplicity.

We show in Fig. 1(a) an HgFET biased into an inversion by a positive gate voltage. The electrons from the source must overcome the Schottky barrier at the source, A, they must traverse the depleted region from the source to channel, B, flow along the channel, traverse the depleted region from channel to drain, C, and finally overcome the drain Schottky barrier, D. For thin, fully depleted Si films, barrier A is the main impediment. For thick, partially depleted films all barriers are important and the drain current is very low and essentially independent of the gate voltage. We discuss thin, fully depleted layers here.

In Fig. 1(b), the negative gate voltage leads to a hole accumulation at the Si/BOX interface and holes throughout the Si film. Since there is no layer depletion, hole flow faces fewer impediments. Nevertheless, the hole barrier height is still important. We describe here how the barrier heights change and their effect on the drain current.

It may not be obvious how there can be barrier heights to electrons and holes in a p-Si sample. We illustrate this in Fig. 2. The band diagrams near the surface are shown in Fig. 2(a) and (b). Fig. 2(a) obtains for zero and positive gate voltages, showing the Schottky barrier source and drain, the hole and

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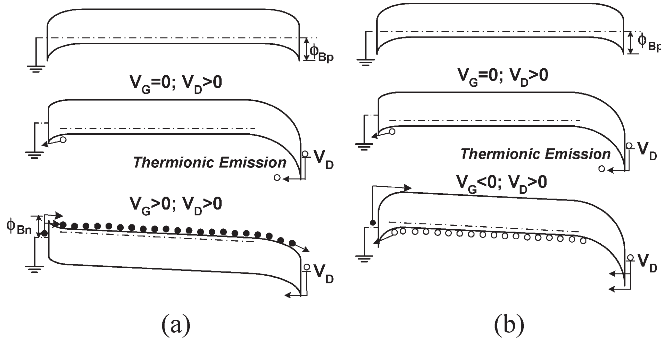

Fig. 2. Schottky MOSFET band diagrams. From top to bottom: (a) $V_G = V_D = 0$; $V_G = 0, V_D > 0$; $V_G > 0, V_D > 0$ and (b) $V_G = V_D = 0$; $V_G = 0, V_D > 0$; $V_G < 0, V_D > 0$.

electron barrier heights, and the space-charge regions. A positive gate voltage leads to an inverted surface. It is obvious from Fig. 2(a) that the electron barrier height (thermionic current) and width (tunnel current) dominate and for appreciable drain to flow, ϕ_{Bn} should be as low as possible. The opposite behavior is shown in Fig. 2(b), where a negative gate voltage accumulates the surface. For current to flow, the hole barrier height should be as low as possible for high-thermionic emission current and/or the space-charge region should be as narrow as possible for high-tunnel current. For appreciable drain current to flow for $V_G > 0$, ϕ_{Bn} should be low while for $V_G < 0$, ϕ_{Bp} should be low, illustrating the conflicting barrier-height requirements for positive and negative gate voltages. We also show possible hole current in Fig. 2(a) by holes injected from the drain and electron current in Fig. 2(b) by electrons from the source. In general, one should expect both hole and electron currents with one or the other dominating.

II. Experimental Results

In this paper, we are concerned with the electron and hole drain currents of the SOI wafers with Si film thicknesses from 19–200 nm and buried oxide (BOX) thicknesses of 100–400 nm. Rinsing the wafer in a dilute buffered oxide etch (BOE) is known to change the Hg/Si barrier height and consequently the drain current. The Hg/n-Si barrier height has been reported to change from 0.47 eV immediately after a dilute HF rinse to 0.72 eV after 40 h in air [10]. We find the electron drain current to be highest immediately after a BOE rinse and then slowly decrease with time over many hours [11]. For drain current measurements, the Si film is etched into islands to reduce leakage currents around the edge of the wafer and through BOX defects. It is then rinsed for 1 min in BOE and the first $I_D{-}V_G$ measurement is made approximately 10 min after the rinse. Then, we measure the curves repeatedly. Source and drain are formed by Hg pressure contacts in the Four Dimensions CV Map 92-B system, using recycling Hg flow through the probe contacts to provide continuous cleaning of the Hg. The Hg probe is made up of a central circular dot serving as the source and a horseshoe-shaped ring as the drain, shown in Fig. 3. The Hg probe contacts the sample facing down, while the metal chuck contacts the wafer back. The Hg probe is lifted after each measurement and the wafer rests on

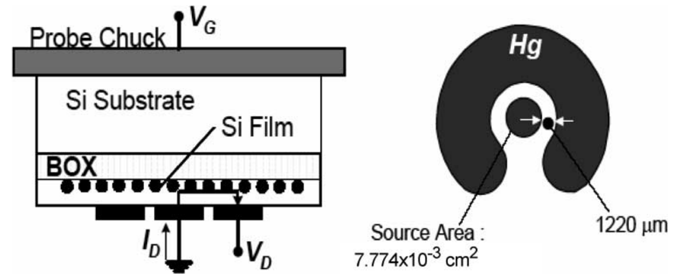

Fig. 3. HgFET and the Hg-probe geometry.

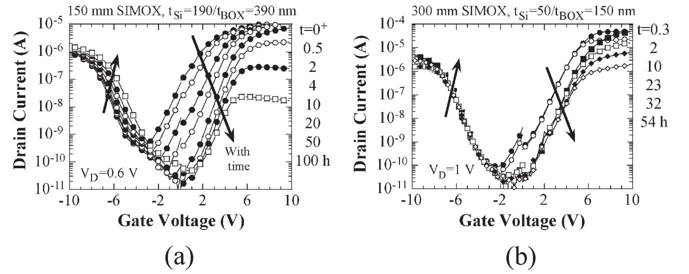

Fig. 4. Hole and electron drain currents versus gate voltage as a function of time following dilute BOE rinse for (a) thick and (b) thin Si films.

the probe station in the room ambient between measurements. The $+V_G$ current not only decreases but shifts along the gate-voltage axis due to threshold-voltage changes. When we rinse the sample again in BOE, the current immediately returns to the original curve.

A. Electron Current

Example electron and hole drain current–gate voltage characteristics are shown in Fig. 4 from immediately after BOE rinse to 100 h later. In contrast to conventional MOSFETs, electron $(+V_G)$ *and* hole $(-V_G)$ drain currents are measured. Both $I_D{-}V_G$ characteristics show subthreshold and above threshold behavior. The electron drain current is initially high with a moderate threshold voltage V_T. With time, I_D decreases and V_T increases. Since the electrons have to overcome the source Schottky barrier and then flow along the channel, one can, to first order, express the electron drain current as a combination channel and Schottky current as

$$I_{D,n} = \frac{I_{\mathrm{n-MOSFET}} I_{\mathrm{Schottky}}}{I_{\mathrm{n-MOSFET}} + I_{\mathrm{Schottky}}} = \frac{I_{\mathrm{n-MOSFET}}}{1 + \frac{I_{\mathrm{n-MOSFET}}}{I_{\mathrm{Schottky}}}}. \quad (1)$$

As ϕ_{Bn} increases, I_{Schottky} and $I_{D,n}$ decrease. We see typically less I_D variation for thin than for thick Si films, seen by comparing Fig. 4(a) and (b). Although these data are for wafers of differing diameter, we observe similar behavior in other wafers from varying manufacturers.

Using the MOSFET charge-sheet drain current model [12] and the usual Schottky-diode equation, gives the $I_D{-}V_G$ curves in Fig. 5(a) with the threshold voltages and barrier heights shown on the figure. Although the curves do not reproduce the experimental data exactly, they show the correct trend. The curves are shifted along the gate voltage axis due to the threshold-voltage changes and along the drain current axis due

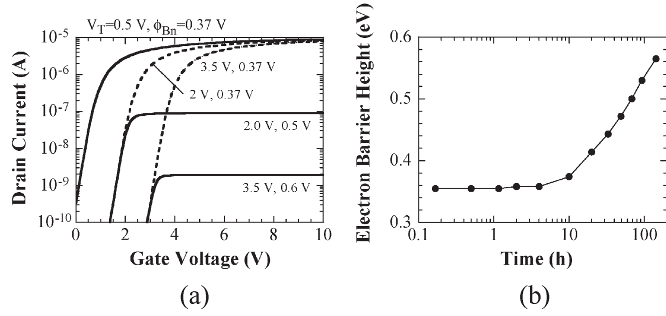

Fig. 5. (a) Calculated electron drain current versus gate voltage curves with (1) for the threshold voltages (V_T) and barrier heights ($\phi_{\rm Bn}$) indicated on the figure. (b) Experimental barrier heights versus time determined from the data in Fig. 4.

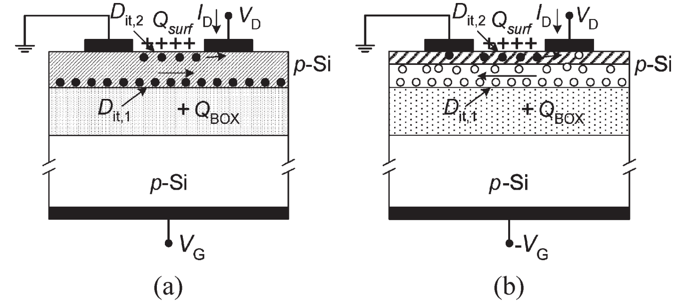

Fig. 6. HgFET cross sections showing (a) electron and (b) hole conduction with the positive surface charge. The arrows indicate the carrier flow directions.

to Schottky barrier height changes. The barrier heights as a function of time after HF rinse in Fig. 5(b) are determined from the data in Fig. 4.

B. Hole Current

We show in Fig. 1(b) a p-HgFET biased into accumulation by a negative gate voltage. There are two significant differences of a p-HgFET from an n-HgFET. One is the hole Schottky barrier height that is highest immediately after BOE rinse and then decreases with time. As reported previously, $\phi_{\rm Bp}$ changes from 0.68 to 0.42 eV with time leading to I_D increase, as seen in Fig. 4. The other is an additional conduction mode—body conduction—as well as an accumulation channel [13].

Fig. 4 show typical I_D-V_G characteristics of p-HgFETs for thin and very thin Si films with identical doping concentrations with the drain current in the thick Si film increasing with time after BOE rinse while the drain current of the very thin Si film changes very little, implying that body conduction in thicker Si films is important for hole currents. For such films, the film contains a bulk region above the accumulation channel that is controlled by the space-charge region width dependence on $Q_{\rm surf}$, the surface-charge density. If the Si film is too thin to contain the bulk region, the current flows mainly through the accumulation channel regardless of a surface charge change with time. Regardless of Si-film thickness, the $-V_G$ drain current always changes less than the $+V_G$ drain current.

C. Threshold Voltage

The Hg–Si barrier height change explains the time-dependent drain current, but does not explain the V_T shift. To understand the V_T change, we propose that the hydrogen in the BOE rinse passivates surface states on the bare Si surface and deposits a positive surface charge $Q_{\rm surf}$ on the H-terminated Si film leading to surface-charge-induced electron channels in Fig. 6(a) and (b), giving an additional drain current in both cases. We only show $Q_{\rm surf}$ in the region between S and D. It exists, of course, over the entire surface. One can think of the semiconductor charge density Q_{s2} induced by $Q_{\rm surf}$ as being similar to the charge density in conventional MOSFETs induced by body bias [14]. With time, $Q_{\rm surf}$ dissipates as the surface oxidizes. As the room temperature, native oxide forms, interface traps at the native oxide/Si interface $D_{\rm it2}$ form. Consequently, the gate voltage depends on the various charge and interface-trap densities (for a fully depleted film with a depleted or inverted top surface) as [2]

$$V_G = \phi_{\rm MS} - \frac{Q_{\rm BOX}}{C_{\rm BOX}} + \left(1 + \frac{C_{\rm it1} + \frac{C_{\rm it2}}{(1+R)}}{C_{\rm BOX}}\right)\phi_s - \frac{Q_{\rm surf} + Q_{s2}}{C_{\rm BOX}(1+R)} - \frac{Q_{s1}}{C_{\rm BOX}} + \frac{Q_{\rm Si}}{2C_{\rm BOX}}\left(1 + \frac{1}{1+R}\right) \quad (2)$$

where $\phi_{\rm MS}$ is the gate/semiconductor work function, $Q_{\rm BOX}$ contains all charges in the BOX, $Q_{\rm surf}$ is the ion charge density on the Si-film surface, Q_{s2} the charge density in the Si film at the surface, Q_{s1} mobile charge density at the Si film/BOX interface, $C_{\rm it1} = qD_{\rm it1}$ and $C_{\rm it2} = qD_{\rm it2}$ the interface-trap capacitances at the bottom and top Si layer surfaces, $Q_{\rm Si} = qN_At_{\rm Si}$ is the depletion charge in the Si film, and $R = C_{\rm it2}/C_{\rm Si}$.

With the doping density in the gate equal to that in the Si film, $\phi_{\rm MS} = 0$. We further assume that at threshold $Q_{s1} \approx 0$ and $\phi_s = 2\phi_F$. With these considerations, the threshold voltage becomes

$$V_T = -\frac{Q_{\rm BOX}}{C_{\rm BOX}} + \left(1 + \frac{C_{\rm it1} + \frac{C_{\rm it2}}{(1+R)}}{C_{\rm BOX}}\right)2\phi_F - \frac{Q_{\rm surf} + Q_{s2}}{C_{\rm BOX}(1+R)} + \frac{Q_{\rm Si}}{2C_{\rm BOX}}\left(1 + \frac{1}{1+R}\right). \quad (3)$$

We further assume that the surface-charge density on the sample deposited during the BOE rinse, induces an equal charge density in the Si film, i.e., $Q_{\rm surf} = -Q_{s2}$. That leaves $C_{\rm it2} = qD_{\rm it2}$ as the only variable.

D. Interface-Trap Density

The MOSFET interface-trap density can be determined from the subthreshold I_D-V_G slope [15]. According to Fig. 4, the n-channel subthreshold slope changes with time, even though we believe that the Si-film/BOX interface properties do not change. If $Q_{\rm surf}$ and $D_{\rm it2}$ in Fig. 6 change with time, then this change should influence the subthreshold behavior, including the slope. From the subthreshold slope we find for the Si/BOX interface $D_{\rm it1} = 6 \times 10^{11}$ cm^{-2}eV^{-1} which is reasonable for a separation by implantation of oxygen (SIMOX) wafer that has not been annealed. After forming gas anneal (450 °C, 30 m) $D_{\rm it1}$ reduces to 2×10^{11} cm^{-2}eV^{-1}. The $Q_{\rm BOX}$ in the

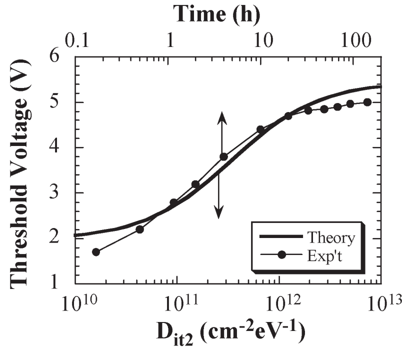

Fig. 7. Threshold voltage versus interface-trap density D_{it2} at the Si surface, theory: $t_{\mathrm{Si}} = 190$ nm, $t_{\mathrm{BOX}} = 390$ nm, $N_A = 10^{15}$ cm^{-3}, $D_{\mathrm{it1}} = 6 \times 10^{11}$ cm^{-2}eV^{-1}, $Q_{\mathrm{BOX}} = 3 \times 10^{11}$ cm^{-2}, experimental data from Fig. 4.

V_T equation is assumed to be located in the BOX at the BOX/Si-film interface.

Equation (3) is plotted in Fig. 7 as a function of D_{it2}. The threshold voltage is straightforward to determine for the higher drain currents, by linear extrapolation, for example [16]. However, as the drain current decreases with time, the linear extrapolation method no longer works. Hence, we used a simple MOSFET/Schottky current model to determine the threshold voltages from the data in Fig. 4 that are also plotted in Fig. 7. Of course, we do not know D_{it2}, hence we plot experimental V_T versus time after BOE rinse. The shape of the curve is similar to theory, confirming that the top surface interface traps D_{it2} are the likely cause of the threshold-voltage variations.

So far we have discussed the effect of Si-film surface charges/traps. It is, of course, possible to change the BOX charge and interface-trap densities by other means. When we exposed SOI wafers to gamma radiation, the $I_D{-}V_G$ characteristics shift to more negative gate voltage due to an increase of positive Q_{BOX} ($\Delta Q_{\mathrm{BOX}}/q = 1.1 \times 10^{11}$ cm^{-2}) assuming all the charge to be located at the Si/BOX interface. There is also a subthreshold slope decrease (subthreshold swing increase) due to increased interface traps (8×10^{11} to 10^{12} cm^{-2}eV^{-1}). We mention it merely to prove that the drain current behavior after BOE rinse is very different from that when the BOX and Si/BOX interface are altered by γ rays, which affect the BOX and the Si/BOX interface, whereas the BOE rinse mainly affects the top Si surface.

The considerations proposed here may also play a role in recent pseudo MOSFET mobility/threshold-voltage measurements, where significant mobility and threshold-voltage changes were observed after ZrO_2, $SrZrO_3$, and SiO_2 deposition on the Si film [17]. The authors attributed the changes to BOX oxygen vacancies and/or interstitial hydrogen. We suggest that changes at the deposited insulator/Si-film interface may be important.

III. Simulation Results

Current–voltage, interface-trap density, and threshold voltage are calculated with SILVACO Atlas [18] for the same configuration as our experimental devices. As mentioned above a dilute BOE rinse not only induces a positive surface charge

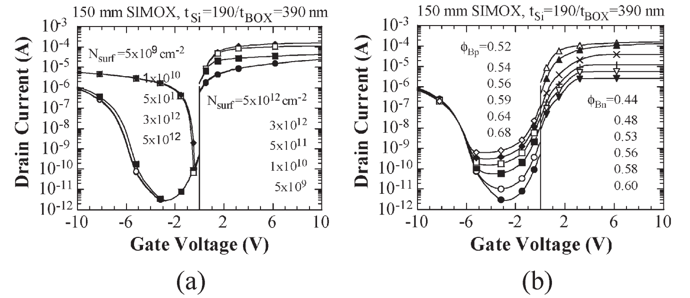

Fig. 8. Simulated drain current versus gate voltage as a function of surface-charge density and barrier height (a) $\phi_{\mathrm{Bp}} = 0.68$ eV, $\phi_{\mathrm{Bn}} = 0.44$ eV; (b) $N_{\mathrm{surf}} = Q_{\mathrm{surf}}/q = 5 \times 10^{12}$ cm^{-2}; $N_A = 10^{15}$ cm^{-3}, $V_D = 0.6$ V.

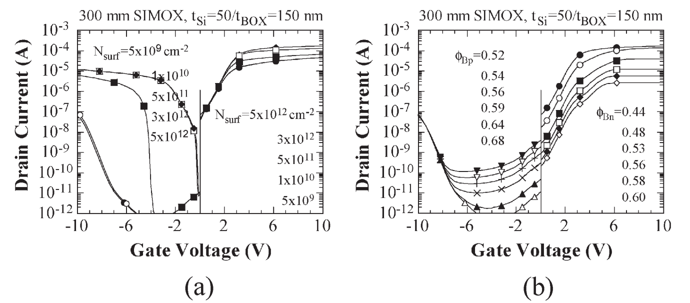

Fig. 9. Simulated drain current versus gate voltage as a function of surface-charge density and barrier height (a) $\phi_{\mathrm{Bp}} = 0.68$ eV, $\phi_{\mathrm{Bn}} = 0.44$ eV; (b) $N_{\mathrm{surf}} = Q_{\mathrm{surf}}/q = 5 \times 10^{12}$ cm^{-2}; $N_A = 10^{15}$ cm^{-3}, $V_D = 0.6$ V.

but also decreases the Hg/Si Schottky barrier height with time. However, we neither know the surface-charge density nor the barrier height nor their changes with time and expect only a qualitative agreement between the simulation and experiment. To study the drain current dependence on the surface-charge density and barrier height, we chose to keep one of these parameters constant while varying the other. We use a positive surface-charge density on the Si-film surface between source and drain contacts varying from 5×10^{12} to 5×10^9 cm^{-2} and electron Hg/Si Schottky barrier heights of 0.44 to 0.6 eV and an interface-trap density at the Si/BOX interface (D_{it1}) of 7×10^{10} cm^{-2}eV^{-1}. The drain current dependence on $N_{\mathrm{surf}} = Q_{\mathrm{surf}}/q$ and ϕ_B is shown in Fig. 8 for thin and Fig. 9 for very thin Si and BOX films.

Initially, the electron drain current is highest due to the surface channel in addition to the main inversion channel as well as the lower barrier height. In time, the surface charge dissipates and the barrier height increases, reducing the current. However, once the barrier height is sufficiently high, the current no longer changes regardless of Q_{surf}, whereas the barrier height continues to affect I_D.

One of the problems in the simulation is that we specify one barrier height (ϕ_{Bn} for electrons or ϕ_{Bp} for holes). However, as illustrated in Fig. 2, both barrier heights play a role and as one increases, the other decreases, assuming $\phi_{\mathrm{Bn}} + \phi_{\mathrm{Bp}} = \mathrm{E}_G$. This is not considered in the simulation program and accounts for the discontinuities at $V_G = 0$. Comparing the effects of the N_{surf} and ϕ_B, we conclude that barrier height exerts a stronger influence on drain current than does surface charge. The influence of Schottky contacts has been discussed by Sato *et al.* [19].

The experimental p-HgFET V_T and I_D changes with time are much less than for n-HgFETs and there is essentially no subthreshold slope change. To verify the body conduction, we varied the Si-film doping concentration and simulated the "immediately after BOE" and "some time later" surface conditions by varying $\phi_{\rm Bp}$ and $Q_{\rm surf}$ (results not shown). The drain current increases with increasing doping concentration and is constant independent of the gate bias for $N_A = 10^{17}$ cm^{-3} even immediately after BOE rinse when the Si surface is covered by a positive charge. However, for very thin Si films, there is no difference of the drain current until $N_A = 10^{16}$ cm^{-3} indicating no part of the body remains neutral due to $Q_{\rm surf}$. Of course, as the doping concentration increases, a neutral region can exist in the Si films. The body conduction portion of the drain current is more substantial in the subthreshold regime than in the above threshold regime, so that before forming an accumulation channel, the drain current flows in the neutral body resulting in lower absolute turn-on voltage.

The simulated drain currents agree reasonably well with experimental data for $Q_{\rm surf}$ = constant, ϕ_B varies. Both electron and hole drain currents depend on the barrier height. The simulations for ϕ_B = constant, $Q_{\rm surf}$ = varying agree qualitatively for $+V_G$, but exhibit large discrepancies for $-V_G$. For example, I_D changes by 6–7 decades as $N_{\rm surf}$ changes from 3×10^{12} to 5×10^{12} cm^{-2}. Clearly, this is unrealistic. Except for these large changes, the simulated curves agree at least qualitatively with experimental data, i.e., I_D (n-channel) decreases with increasing $\phi_{\rm Bn}$ and decreasing $Q_{\rm surf}$. The I_D decrease with $\phi_{\rm Bn}$ is obvious, because higher barriers allow less current. We believe that the I_D reduction with decreasing $Q_{\rm surf}$ is the result of a reduction of the surface-charge-induced electron channel. The hole drain current is less sensitive to $Q_{\rm surf}$ and $\phi_{\rm Bp}$ for $V_G < -6$ V, as we also observe experimentally. We do not understand the high simulated hole currents for $N_{\rm surf} < 3 \times 10^{12}$ cm^{-2}. They may be an artifact of the simulation; certainly the experimental data do not exhibit this behavior. It may be that $\phi_{\rm Bp}$ and $Q_{\rm surf}$ are not recovered to their initial "before BOE rinse" condition. This is consistent with Hg/Si Schottky diode barrier height measurements, where the Hg/H-p-Si ideality factor did not recover to unity a long time after HF rinse whereas the Hg/H-n-Si did [10]. The simulations show a lower surface-charge density leading to the higher drain current with surface-charge dissipation adding body conduction to p-channel conduction. Further work is in progress to elucidate the mechanisms not understood at this time. Without additional definitive information, we do not wish to speculate about the nature of the current discrepancies.

A. Interface-Trap Density

The drain current in the subthreshold and above threshold regimes is influenced by the surface charge and the barrier height. We measured and simulated $D_{\rm it1,eff}$, the effective interface-trap density at the Si/BOX interface. The experimental interface-trap density versus time after BOE rinse and the simulated $D_{\rm it1,eff}$ versus $\phi_{\rm Bn}$ and $Q_{\rm surf}$ are shown in Fig. 10. $D_{\rm it1,eff}$ is determined from the subthreshold slope. The interface-trap density is designated as $D_{\rm it1,eff}$ here because it is not the true interface-trap density.

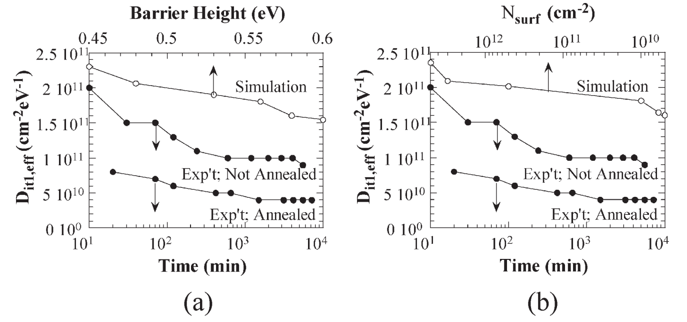

Fig. 10. Simulated interface-trap density versus barrier height, and experimental interface-trap density versus time. (a) $N_{\rm surf}$ varies from 5×10^{12} to 5×10^9 cm^{-2} as barrier height varies from 0.45 to 0.6 eV. (b) Barrier height varies from 0.45 to 0.6 eV as $N_{\rm surf}$ varies from 5×10^{12} to 5×10^9 cm^{-2}; $t_{\rm Si} = 190$ nm, $t_{\rm BOX} = 390$ nm, $N_A = 10^{15}$ cm^{-3}; experimental data from Fig. 3.

Although there is some discrepancy between simulation and experimental data, the trend is the same. As a result of the simulation and experiment, we propose that the positive surface charge from the BOE rinse forms a parasitic surface electron channel at the top surface of the Si film immediately after rinse and gives a low-electron barrier height, inducing a coupling between the upper Si-film surface and Si-film/BOX interface similar to a fully depleted SOI MOSFET. The true $D_{\rm it1}$ is obtained for $t \to \infty$, i.e., when the surface charge is largely dissipated.

IV. SUMMARY

We illustrated the effect of a dilute BOE rinse on SOI HgFET I_D–V_G characteristics, attributing the n-channel drain current decrease to a threshold voltage shift due to surface charges and interface traps at the Si-film surface and to Hg/Si Schottky barrier height changes due to interface traps at the Hg/Si interface. Both surface-charge density and threshold voltage vary in time after the BOE rinse leading to n-HgFET and p-HgFET drain current changes. The drain current for n-HgFETs decreased and for p-HgFETs it increased. The behavior is very different from the case where the charges/traps in the BOX and at the Si/BOX interface are altered. Furthermore, surface charge and Si-film surface interface traps influence the Si/BOX interface trap density extraction.

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