Analytical Modeling of the Partially-Depleted SOI MOSFET

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***Abstract*—An analytical model for the partially-depleted (PD) silicon-on-insulator (SOI) MOSFET above threshold was developed. In contrast to previous models, this model includes front–back interface coupling with all the possibilities associated with it (accumulated, neutral, and depleted back interface). The model applies to tied-body as well as floating-body devices; however, thermal and edge effects are neglected. Interface coupling and floating-body effects are integrated together in a new, "unified" algorithm. The "pseudo-two-dimensional" approach (which was used successfully to model lateral fields in bulk-Si devices) is extended to SOI devices. The model is extremely physical and thus highly predictive. Good agreement with experiment was obtained over a wide range of channel lengths and back gate voltages. Because of the model's neglect of thermal effects, however, disagreement was observed at high current levels. A brief physical interpretation of the results is also presented.**

***Index Terms*—Floating body, interface coupling, partially depleted, SOI MOSFET model.**

I. Introduction

FULLY-DEPLETED (FD) SOI MOSFETs have demonstrated several advantages in addition to the traditional advantages of SOI devices [1]. These include higher current drive, higher transconductance, and smaller subthreshold swing. FD devices, however, suffer from a serious problem. Because of front–back interface coupling, the threshold voltage, V_T, depends on Si film thickness. Since film thickness is difficult to control across the wafer, V_T becomes nonuniform across the wafer [2]. For this reason, there has been a growing interest in partially-depleted (PD) SOI MOSFETs lately [3], [4].

The purpose of this work is to develop an analytical model for the PD SOI MOSFET in the above-threshold regime. Most of the previous work in SOI MOSFET modeling has focused on FD devices [5], [6]. Furthermore, the few PD models that exist today [7], [8] do not adequately account for interface coupling even though it *does* occur in PD devices. Our model includes interface coupling with all the possibilities associated with it (accumulated, neutral, and depleted back Si surface). Our model applies to tied-body as well as floating-body devices; however, thermal and edge effects are neglected. We integrate interface coupling and floating-body effects in a new, "unified" algorithm. The algorithm is "unified" since it models floating-body effects by accounting for the interaction between body-source voltage, V_{BS}, and *all* other device parameters (e.g., the charge condition of the back interface, electric field, multiplication factor, channel charge, etc.). Our model is extremely physical and thus highly predictive.

Floating-body effects appear as a slightly higher current in the linear region and early in saturation, a "kink" later in saturation, and eventually premature breakdown. The mechanisms responsible for floating-body effects are explained in detail in other publications [9], [10]. The next section explains interface coupling and all the possibilities associated with it. Section III presents the model formulation. Section IV describes our algorithm. Section V presents the experimental support, and finally Section VI presents a brief discussion of the results.

II. Interface Coupling

Consider a PD SOI MOSFET with a drain-to-source voltage $V_{DS} = 0$ and a *front* gate voltage $V_{GS} > V_T$. Depending on how V_{GBb} (the back-gate voltage with respect to the neutral body) compares with the back Si surface flatband voltage, V_{FBb}, there are three possible cases [11]. If $V_{GBb} = V_{FBb}$, the back surface is neutral (Case I). If $V_{GBb} > V_{FBb}$, the back surface is depleted (Case II). Inversion of the back surface is avoided in most practical applications and thus will be neglected in this work. Finally, if $V_{GBb} < V_{FBb}$, the back surface is accumulated (Case III).

Obviously the front and back Si/SiO_2 interfaces are decoupled over the entire channel length in the three cases described above. When V_{DS} is raised to a value below V_{Dsat}, however, the possibility of interface coupling increases with position along the channel. In other words, the latter part of the channel could have coupled interfaces while the earlier part could have decoupled ones. This is because of the rise of the channel voltage, $V_{CS}(y)$, with position y and the concomitant increase of the front depletion region depth. When V_{DS} exceeds V_{Dsat}, the channel is divided into a source section and a drain section [12]. Since interface coupling is due to a field that is perpendicular to the two interfaces (i.e., a vertical field), the possibility of coupling increases with position only in the source section. In the drain section, the possibility of coupling does not change since the field direction there is practically lateral.

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In light of the interface coupling concepts discussed above, when V_{DS} is raised from zero toward V_{Dsat}, several "scenarios" are possible in each of the three cases. For case I, a channel voltage of V_f (the calculation of which is based on electrostatic analysis) is needed to deplete the full thickness of the Si film and thus couple the two interfaces. Therefore, as V_{DS} is raised from zero toward V_{Dsat}, there are two possible scenarios. First, if V_{DS} reaches V_{Dsat} before it reaches V_f (i.e., $V_{Dsat} < V_f$), then at $V_{DS} = V_{Dsat}$ the two interfaces will be decoupled over the entire channel length. Second, if V_{DS} reaches V_f before it reaches V_{Dsat} (i.e., $V_f < V_{Dsat}$), then the two interfaces become coupled at the drain end of the channel (for $V_{DS} = V_f$). And as V_{DS} rises from V_f toward V_{Dsat}, the point where the two interfaces become coupled retreats from the drain end of the channel toward the source. Thus, at $V_{DS} = V_{Dsat}$, the two interfaces are decoupled in the earlier part of the channel and coupled in the latter one. In either scenario, the device is bulk-Si-like over the part of the channel with decoupled interfaces and FD-SOI-like over the part with coupled interfaces. Any increase of V_{DS} beyond V_{Dsat} is immaterial as far as interface coupling is concerned, because all such an increase does is create the drain section of the channel where the field direction is practically lateral.

In Case II, a channel voltage of V_{fd} (the calculation of which is based on electrostatic analysis) is needed to cause the front depletion region to extend to the back depletion region and thus cause the full thickness of the Si film to be depleted. Like Case I, Case II has two possible scenarios associated with it. First, if $V_{Dsat} < V_{fd}$, then at $V_{DS} = V_{Dsat}$ the two interfaces are decoupled over the entire channel length. Second, if $V_{fd} < V_{Dsat}$, then at $V_{DS} = V_{Dsat}$ the two interfaces will be decoupled in the earlier part of the channel and coupled in the latter one.

Case III is a little more complicated than Cases I and II. In Case III, a channel voltage V_f is required to deplete the full thickness of the Si film and thus cause the channel to start "communicating" with the back accumulation layer. Similarly, a channel voltage of V_{fa} (the calculation of which is based on electrostatic analysis) is needed for the back accumulation layer to disappear altogether. Obviously, V_{fa} is always larger than V_f. Therefore, as V_{DS} is raised from zero toward V_{Dsat}, there are *three* possible scenarios. First, if V_{DS} reaches V_{Dsat} before it reaches V_f (i.e., $V_{Dsat} < V_f$), then at $V_{DS} = V_{Dsat}$, a neutral region will exist below the entire channel length and the two interfaces will be decoupled over the entire channel length. Second, if V_{DS} reaches V_f before it reaches V_{Dsat} (i.e., $V_f < V_{Dsat}$), the channel will start communicating with the back accumulation layer at the drain end of the channel (for $V_{DS} = V_f$). And as V_{DS} rises beyond V_f, the point where the channel starts communicating with the back accumulation layer retreats from the drain end of the channel toward the source. If V_{DS} reaches V_{Dsat} before it reaches V_{fa} (i.e., $V_{Dsat} < V_{fa}$), then at $V_{DS} = V_{Dsat}$, the two interfaces will be decoupled in the earlier part of the channel and coupled with a back accumulation layer in the latter part of the channel. Third, if V_{DS} reaches V_{fa} before it reaches V_{Dsat} (i.e., $V_{fa} < V_{Dsat}$), then the back accumulation layer totally disappears at the drain end of the channel (for $V_{DS} = V_{fa}$). As V_{DS} rises from V_{fa} toward V_{Dsat}, the point where the channel starts to communicate with the back accumulation layer and where the back accumulation layer totally disappears, retreat toward the source. Thus, at $V_{DS} = V_{Dsat}$, the two interfaces are decoupled in the early part of the channel, coupled with a back accumulation layer in the middle part, and totally coupled in the late part.

III. Model Formulation

A. Linear Region Modeling (Drain-to-Source Voltage $\leq V_{Dsat}$)

1) Formulation of Drain Current Equations: To derive equations for the drain current applicable to the three cases (I, II, and III) and the possible scenarios described in the last section, we modified Tsividis' bulk-Si MOSFET derivation [13] to fit each of the scenarios. Consider Case I. In the first scenario, the device is bulk-Si-like over the entire channel length regardless of V_{DS}. Thus, the bulk-Si equation is used. In the second scenario, the device is bulk-Si-like over the entire channel length for $V_{DS} \leq V_f$. For $V_{DS} > V_f$, however, the device is bulk-Si-like over the earlier part of the channel (V_{CS}: 0 to V_f) and FD-SOI-like over the latter part (V_{CS}: V_f to V_{DS}). Therefore, the bulk-Si equation is used for $V_{DS} \leq V_f$. And for $V_{DS} > V_f$, the derivation is modified yielding

$$I_D = \frac{W}{L}\frac{1}{\left(1+\frac{1}{L}\left[\frac{V_f}{E_c}+\frac{V_{DS}-V_f}{E_{cfd}}\right]\right)} \cdot\left\{\mu_{\text{eff}}\int_0^{V_f}(-Q_I)dV_{CS}+\mu_{fd\text{eff}} \cdot\int_{V_f}^{V_{DS}}(-Q_{Ifd})dV_{CS}\right\} \tag{1}$$

where $\mu_{fd\text{eff}}$, $(-Q_{Ifd})$, and E_{cfd} are the effective mobility, channel charge per unit area, and critical field in the latter part of the channel, respectively. E_{cfd} is given by $E_{cfd} = 2|v_{sat}|/\mu_{fd\text{eff}}$, where v_{sat} is the saturation velocity of channel electrons. Similar definitions apply to μ_{eff}, Q_I, and E_c; however, these parameters are associated with the earlier part of the channel.

Case II is identical to Case I except that V_f is replaced by V_{fd}. The equations for Case III are similar to those for Cases I and II; however, Case III is more complicated than Cases I and II since it has three scenarios associated with it as opposed to just two.

2) Calculation of V_{Dsat}: V_{Dsat} is calculated following Tsividis [13], who showed that saturation of the I_D–V_{DS} curves is caused by velocity saturation at the drain-end of the channel. We modified Tsividis' calculation as needed to fit each of the scenarios described in the last section.

3) Electrostatics and Mobility: We used the electrostatic analysis in [6] for the FD SOI electrostatic parameters (Q_{Ifd}, Q_{Ifda}, V_{fa}) and the one in [13] for the bulk-Si electrostatic parameters (Q_I, V_f, V_{fd}). We based our calculation of effective mobility on the "universal" mobility relationship, valid in both bulk-Si and FD SOI MOSFET's [14], [15].

B. Saturation Region Modeling (Drain-to-Source Voltage $> V_{Dsat}$)

As in bulk-Si MOSFETs, the drain current in saturation is obtained using the linear region equations presented in Section III-A-1 with L replaced with $(L - \Delta L)$ and V_{DS} replaced with V_{D1} [12], [16], where V_{D1} is the channel voltage at the boundary between the source and drain sections, and ΔL is the length of the drain section. We set up a system of two equations to solve for V_{D1} and ΔL [16]. The first equation is the same as the ones used to calculate V_{Dsat} except for the replacement of V_{Dsat} with V_{D1} and L with $(L - \Delta L)$. The second equation is obtained using the "pseudo-two-dimensional" approach, which we extended from bulk-Si [12] to SOI MOSFETs. This is the subject of a future publication. Since our experimental devices have lightly-doped drains (LDDs), we included the depletion region in the n^- part of the drain in our saturation region modeling.

C. Modeling of Generation Currents and Body/Source Diode Current

The generation current due to impact ionization at the drain, I_{gii}, is given by

$$I_{gii} = (M-1)I_{ch} \tag{2}$$

where I_{ch} is the channel current and M is the multiplication factor. $(M-1)$ is given by [12]

$$(M-1) \cong \frac{A_i}{B_i}(V_{DS} - V_{Dsat}) \exp\left(\frac{-B_i\lambda}{V_{DS} - V_{Dsat}}\right) \tag{3}$$

where A_i and B_i are electrical parameters in our model, and λ is a parameter dependent on physical device parameters such as gate oxide thickness and doping density. λ is associated with the pseudo-2-D approach. It is important to note that λ and V_{Dsat} change depending on which scenario is true, which makes $(M-1)$ dependent on scenario. Since our experimental devices have LDDs, we added a second term to the right-hand side of equation (3) to account for impact ionization in the n^- part of the drain.

We use the following model for the thermal generation current in the drain/body diode

$$I_{gth} = A_{BD}C_oV_{DB}^r \tag{4}$$

where V_{DB} is the drain-body voltage. C_o and r are treated as electrical parameters in our model. We use $A_{BD} = Wt_{si}$.

We use the following model for I_{BS}, which is the forward-bias current in the body/source diode

$$I_{BS} = A_{BS}J_s\left[\exp\left(\frac{qV_{BS}}{n_1kT}\right) - 1\right] + A_{BS}J_r\left[\exp\left(\frac{qV_{BS}}{n_2kT}\right) - 1\right] \tag{5}$$

where J_s, J_r, n_1, and n_2 are electrical parameters. A_{BS} is the area of the body/source diode.

IV. Algorithm to Generate I_D–V_{DS} Characteristics

The algorithm is divided into two phases. Phase 1 is concerned with the device *prior* to the activation of the parasitic BJT (the linear region and the kink), while Phase 2 is concerned with the device *after* the activation of the parasitic BJT (premature breakdown).

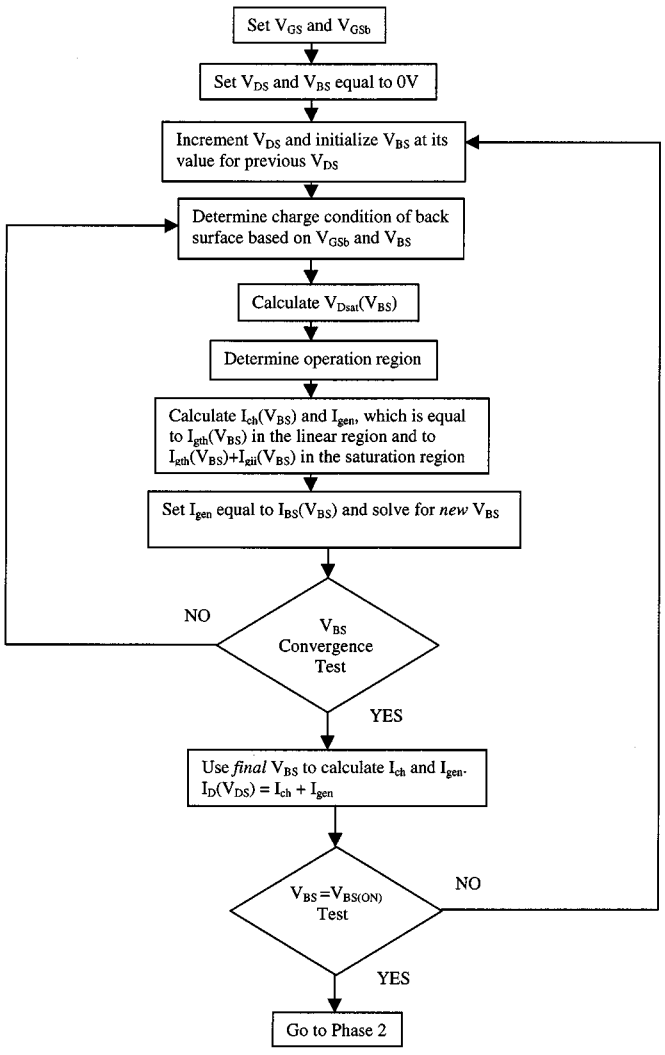

Fig. 1. Algorithm to generate I_D–V_{DS} characteristics (Phase 1).

The flowchart for Phase 1 is shown in Fig. 1. The fundamental concept of Phase 1 can be explained as follows. For a given biasing condition (V_{GS}, V_{GSb}, and V_{DS}), V_{BS} is initialized and the charge condition of the back Si surface is tested by comparing $V_{GBb}(= V_{GSb} + V_{SB})$ with V_{FBb}. If the back surface is depleted, $V_{fd}(V_{BS})$ is calculated; if it is neutral, $V_f(V_{BS})$ is calculated; and if it is accumulated, $V_f(V_{BS})$ and $V_{fa}(V_{BS})$ are calculated. Then, for any charge condition, the following is done (we use the depleted case as an example). The first scenario is assumed to be true, and $V_{Dsat}(V_{BS})$ is calculated. If $V_{Dsat}(V_{BS}) \leq V_{fd}(V_{BS})$, then indeed the first scenario is true. However, if $V_{Dsat}(V_{BS}) > V_{fd}(V_{BS})$, then the second scenario is true, and thus $V_{Dsat}(V_{BS})$ is recalculated based on the second scenario. Then, the operation region is determined by comparing the applied V_{DS} with $V_{Dsat}(V_{BS})$. In either operation region, I_{ch} and I_{gen} are calculated using the *current* V_{BS}. In the saturation region, I_{ch} is calculated based on the appropriate scenario. In the linear region, I_{ch} is calculated as

follows. If the first scenario is true, then the bulk-Si equation is used. If the second scenario is true, then the bulk-Si equation is used if $V_{DS} \leq V_{fd}(V_{BS})$, and equation (1) is used if $V_{DS} > V_{fd}(V_{BS})$. The difference between the two operation regions as far as I_{gen} is concerned is as follows. In the linear region, $I_{gen} = I_{gth}$; while in the saturation region, $I_{gen} = I_{gth} + I_{gii} \cong I_{gii}$ (the appropriate scenario is taken into account when calculating I_{gii}). The next step is to set I_{gen} equal to $I_{BS}(V_{BS})$ and solve the resulting equation for a *new* V_{BS}. Then, V_{BS} is tested for convergence. If V_{BS} fails the convergence test, the above steps (starting with testing the charge condition of the back surface) are repeated using the *new* V_{BS}. The program iterates until V_{BS} converges. Once V_{BS} converges, the *final* V_{BS} is used to calculate I_{ch} and I_{gen}. Then, $I_D(V_{DS})$ is calculated using $I_D = I_{ch} + I_{gen}$. From the above, it is clear that our algorithm integrates interface coupling (with all the possible scenarios described previously) and floating body effects in a large, "unified" scheme.

To generate an I_D–V_{DS} curve, V_{GS} and V_{GSb} are held constant and V_{DS} is swept, i.e., incremented by small amounts starting at zero volt. Every time V_{DS} is incremented, V_{BS} is initialized at the previous value of V_{BS} (the *final* V_{BS} obtained for the previous V_{DS}), and the procedure is performed. V_{DS} is swept until V_{BS} reaches the body/source diode turn-on voltage, $V_{BS(ON)}$. At this point, V_{BS} is "pinned" at $V_{BS(ON)}$, and I_{ch} is "pinned" at the value corresponding to $V_{BS(ON)}$. Phase 2 is then used to generate the rest of the I_D–V_{DS} curve. $V_{BS(ON)}$ and I_{ch} corresponding to it are substituted in Phase 2.

Phase 2 is given by the following equation, which is obtained by analyzing the equivalent circuit of the device with the parasitic BJT activated.

$$I_D = \frac{MI_{ch}}{1 - \beta(M-1)}. \tag{6}$$

We treat the gain of the parasitic BJT, β, as an electrical parameter.

V. Experimental Support

The devices utilized for experimental support were provided by Motorola. They had a front oxide thickness of 10 nm, a Si film thickness of 100 nm, a BOX thickness of 370–380 nm. The Si film had a doping density $N_A = 2 \times 10^{17}$ cm^{-3}, and the Si substrate had a doping density $N_{SUB} = 1 \times 10^{15}$ cm^{-3}. An n$^+$ poly-Si layer formed the front gate. The devices had LDDs. The width of the n$^-$ part of the drain was equal to that of the spacer (0.2 μm). The n$^-$ part of the drain had a doping density $N_{\text{LDD}} = 1 \times 10^{19}$ cm^{-3}. Both H-gate (tied-body) and floating-body layouts were available, and the SOI wafers were made using wafer bonding technology.

We obtained the physical parameters in our model (e.g., doping densities and device dimensions) directly from process information. The electrical parameters in our model have a strong physical meaning, and we obtained them as follows. We used $v_{sat} = 1 \times 10^7$ cm/sec, obtained from other published works [17], [18]. We extracted μ_o and α_o, which appear in the "universal" mobility relationship, by characterizing μ and μ_{fd} in a tied-body (H-gate) device. The diode parameters were extracted by measuring the current-voltage characteristic of the body/source (or body/drain) diode in a tied-body device. Unfortunately, we were unable to detect extremely low currents, such as the reverse-bias leakage current and the recombination current at small forward bias.

Consequently, we had to neglect I_{gth} and the recombination component of our I_{BS} model. We expect the impact of the above simplifications to be minor since the currents we neglected are very low. We extracted A_i and B_i by characterizing $(M-1)$ in a tied-body device. We fixed A_i at the typical value of 2.45×10^6 cm^{-1} and adjusted B_i at 3.6×10^6 V/cm to fit the experimental data. We extracted $V_{BS(ON)}$ from the body/source diode characteristic as $V_{BS(ON)} = 0.75$ V. We assume β is a function only of device dimensions, material quality, and V_{GSb}. To extract β for a given channel length and V_{GSb}, we measured an I_D–V_{DS} curve at a given V_{GS}. We then used (6) to fit the premature-breakdown part of the curve with β as a fitting parameter. As an example, at $L = 2$ μm and $V_{GSb} = -6$ V, we extracted a β of 11.1. In our extraction of electrical parameters, we tried to minimize thermal effects. For example, to extract the impact ionization parameters, we minimized the currents by using the longest-channel device (5 μm) and fairly low gate voltages.

We now verify our model by comparing with experimental results obtained from floating-body devices. We obtained results for the channel lengths: $L = 5$ μm, 2 μm, and 0.8 μm and width W of 25 μm. At each L, we obtained I_D–V_{DS} characteristics at $V_{GSb} = +5$ V and -6 V. V_{FBb} is about -2.8 V in our experimental devices. Thus, $V_{GSb} = +5$ V and -6 V correspond to a depleted back surface (Case II) and an accumulated back surface (Case III), respectively.

The emphasis in floating-body devices is on the prediction of the kink and premature breakdown, both of which occur in the saturation region. Due to the measurement limitations mentioned above, the prediction of the *slight* floating-body-induced enhancement of I_D in the linear region is not possible. Therefore, we limit our comparison between model and experiment to the saturation region in floating-body devices. Our goal was to ascertain that discrepancies in the saturation region were indeed caused by inaccuracies in saturation-region modeling rather than inaccuracies in the relatively unimportant linear region (e.g., inaccuracies due to the model's neglect of edge effects). To achieve this goal, we calibrated the width W such that the calculated and measured values of I_D agreed perfectly at the onset of saturation, i.e., at $V_{DS} = V_{Dsat}$. We validated our linear-region modeling by obtaining good agreement between model and experiment in H-gate devices (with $V_{BS} = 0$ V) over a wide range of channel lengths (5 to 0.8 μm) and back gate voltages ($+5$ V to -6 V). The model's neglect of edge effects is immaterial in H-gate devices since H-gate devices are edgeless.

We present results for the 5 μm and 2 μm devices (thermal effects were too strong in the 0.8 μm device due to the high I_D). As shown in Figs. 2–5, generally our model predicts the kink and premature breakdown reasonably. Disagreements between model and experiment can be classified into two categories.

1) Overestimation of the kink due to our model's neglect of thermal effects and the concomitant negative differential

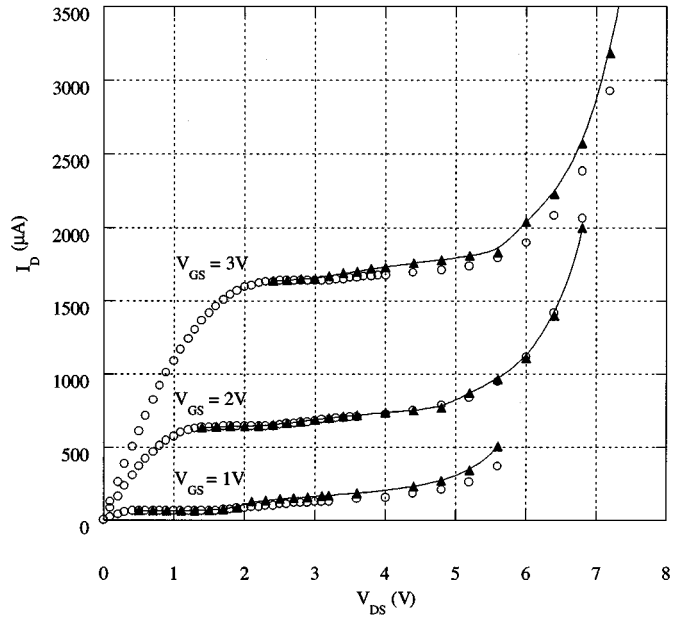

Fig. 2. I_D–V_{DS} characteristics: experiment (open circles) versus model (solid triangles) for $W/L = 25$ μm/5 μm at $V_{GSb} = +5$ V.

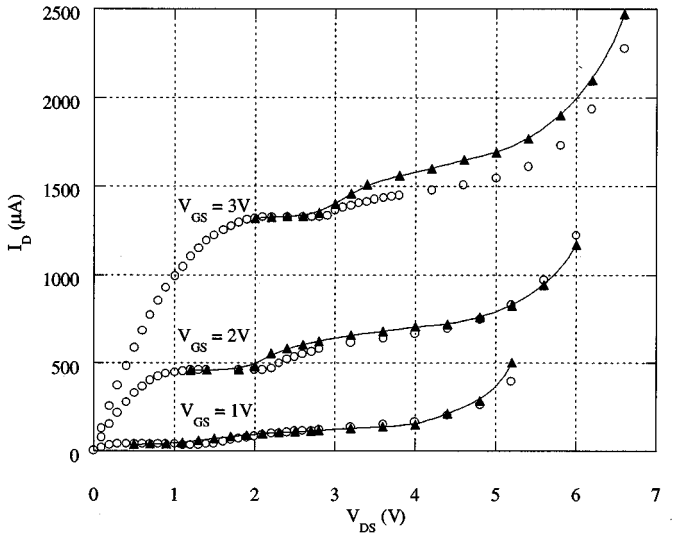

Fig. 3. I_D–V_{DS} characteristics: experiment (open circles) versus model (solid triangles) for $W/L = 25$ μm/5 μm at $V_{GSb} = -6$ V.

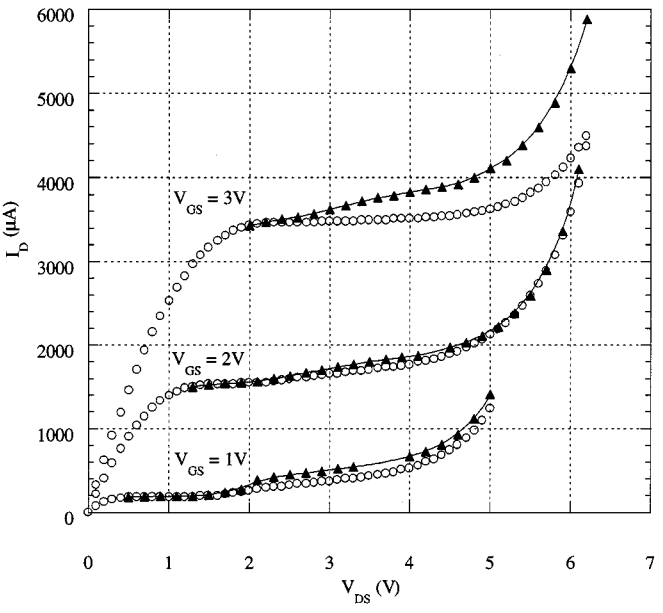

Fig. 4. I_D–V_{DS} characteristics: experiment (open circles) versus model (solid triangles) for $W/L = 25$ μm/2 μm at $V_{GSb} = +5$ V.

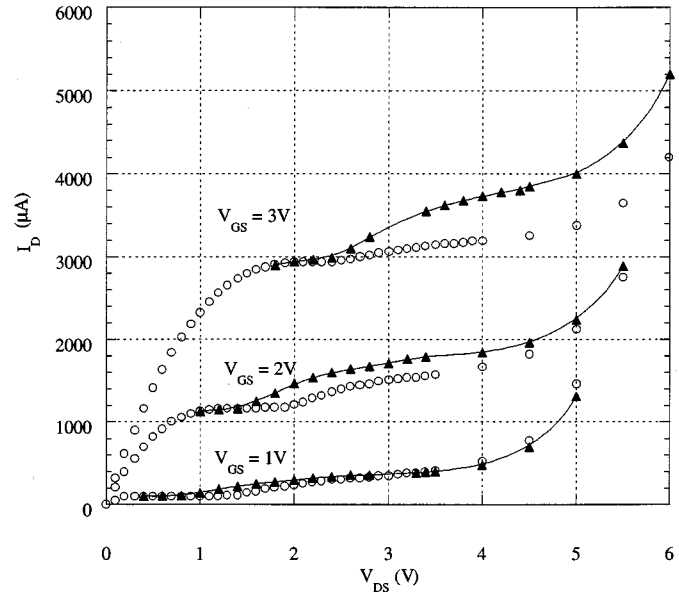

Fig. 5. I_D–V_{DS} characteristics: experiment (open circles) versus model (solid triangles) for $W/L = 25$ μm/2 μm at $V_{GSb} = -6$ V.

conductance. This disagreement is expected, and it appears only at high current levels (in the 0.8 μm device especially at $V_{GS} = 2$ V and 3 V and in the 2 μm device at $V_{GS} = 3$ V). Using thermal models, we calculated $R_{th} \cong 25$ K/mW for our experimental devices, which is typical of SOI devices [19].

2) Overestimation of the kink when the first scenario is true, i.e., when the device is bulk-like over the entire channel length. This is seen in the 2 μm device with $V_{GSb} = -6$ V at $V_{GS} = 1$ V and 2 V and slightly in the same device with $V_{GSb} = +5$ V at $V_{GS} = 1$ V.

Evidently, our model overestimates E_m and thus $(M-1)$ in the first scenario. We attribute this to inaccuracies in the analytical expression for λ in the first scenario. Generally, analytical expressions for λ are in slight disagreement with those obtained experimentally (using substrate current measurements in bulk Si devices) and from 2-D simulations [20]. Using MEDICI simulations, we showed that this is especially true when the first scenario is true. Since $(M-1)$ is exponentially dependent on λ, a slight error in λ could result in a noticeable error when modeling the kink. Further work is needed to improve the accuracy of λ. We believe that the expression for λ should not be changed.

Rather, the spreading parameter that appears in the expression for λ should be correlated better to MEDICI simulations when the first scenario is true. We plan discuss this in a future publication.

VI. Discussion

Figs. 2–5 illustrate several trends associated with the kink. For a given L and V_{GSb}, the kink becomes less pronounced and starts at a higher V_{DS} as V_{GS} increases. This trend is caused by the increase of V_{Dsat} with V_{GS}, which lowers E_m and thus lowers $(M-1)$. Although I_{ch} increases with V_{GS}, the decrease of $(M-1)$ dominates causing $I_{gii} = (M-1)I_{ch}$ to decrease.

Figs. 2–5 also show that for a given L and V_{GS}, the kink becomes less pronounced and starts at a higher V_{DS} as V_{GSb} increases. There are two reasons for this trend. First, V_{Dsat} increases as V_{GSb} increases (due to the increase in channel charge as the device approaches FD SOI, *without* a back accumulation layer, and deviates from bulk-Si) causing E_m to decrease. This lowers $(M-1)$ and I_{gii}. Second, I_D in a PD SOI device becomes less sensitive to V_{BS} the closer the device is to a FD SOI device *without* a back accumulation layer, i.e., as V_{GSb} increases. It is well known that the body charge (and thus the channel charge) in such a device is independent of V_{BS} [21]. The body charge is actually "pinned" at $-qN_At_{si}$.

Finally, Figs. 2–5 show that for a given V_{GS} and V_{GSb}, the kink starts at a lower V_{DS} as L decreases, because a shorter L results in a lower V_{Dsat} and thus a higher E_m and a higher $(M-1)$. The reduction in L also results in an increase in I_{ch}, although not as strong as the increase in $(M-1)$. The increase in $(M-1)$ and I_{ch} as L becomes shorter causes I_{gii} to increase. It was shown, however, that when L is sufficiently short for charge sharing to become significant, the kink becomes less pronounced [22]. This is because charge sharing reduces the sensitivity of the body charge (and thus channel charge) to V_{BS}. This phenomenon is not investigated here since our model does not include charge sharing.

VII. Conclusion

An analytical model for the PD SOI MOSFET above threshold was developed. In contrast to previous models, this model includes front–back interface coupling with all the possibilities associated with it (accumulated, neutral, and depleted back interface). Interface coupling and floating-body effects were integrated together in a new, "unified" algorithm. Thermal and edge effects, however, were neglected. The pseudo-2-D approach was extended from bulk-Si to SOI MOSFET's. The model is extremely physical and thus highly predictive. Good agreement with experiment was obtained over a wide range of channel lengths and back gate voltages. Disagreement was observed, however, at high current levels due to the model's neglect of thermal effects. A brief physical interpretation of the results was presented.

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