Degradation of Thin Tunnel Gate Oxide Under Constant Fowler–Nordheim Current Stress for a Flash EEPROM

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Abstract— **The degradation of thin tunnel gate oxide under constant Fowler–Nordheim (FN) current stress was studied using flash EEPROM structures. The degradation is a strong function of the amount of injected charge density (Q_{inj}), oxide thickness, and the direction of stress. Positive charge trapping is usually dominant at low Q_{inj} followed by negative charge trapping at high Q_{inj}, causing a turnaround of gate voltage and threshold voltage. Interface trap generation continues to increase with increasing stress, as evidenced by subthreshold slope and transconductance. Gate injection stress creates more positive charge traps and interface traps than does substrate injection stress. Oxide degradation gets more severe for thicker oxide, due to more oxide charge trapping and interface trap generation by impact ionization. A simple model of oxide degradation and breakdown was established based on the experimental results. It indicates that the damage in the oxide is more serious near the anode interface by impact ionization and oxide breakdown is also closely related to surface roughness at the cathode interface. When all the damage sites in the oxide connect and a conductive path between cathode and anode is formed, oxide breakdown occurs. The damage is more serious for thicker oxide because a thicker oxide is more susceptible to impact ionization.**

Index Terms— **Charge injection, dielectric breakdown, EPROM, impact ionization, leakage current, MOS devices, stress measurement, tunneling.**

I. INTRODUCTION

THE degradation of the thin gate oxide under high-field stress is of great importance to MOS devices. As the gate oxide thickness is reduced in order to achieve better MOS device performance, the oxide electric field continues to increase. With these increasing electric fields many degradation mechanisms begin to emerge. Primary among these are interface trap generation and charge trapping in the SiO_2, both or either of which can cause severe degradation of the device performance and of its operating life.

Particularly, the integrity and reliability of the thin tunnel gate oxide are essential for flash EEPROM devices [1]–[3]. Their operation involves the transfer of charge through the oxide between a silicon (Si) substrate and a floating polysilicon (poly-Si) gate. Fowler–Nordheim (FN) tunneling has been one of the main mechanisms for programming and erasing the memory cells. Unfortunately, the current through the oxide degrades the quality of the oxide, causing drift in the threshold voltage (V_T), reduction of transconductance (g_m), increase of subthreshold current swing, increase of stress-induced oxide leakage current, and eventual oxide breakdown. Therefore, the problems associated with the charge flow through the oxide are of primary concern for flash memories.

In order to realize highly reliable performance of the flash EEPROM memory cell, the degradation mechanism of the oxide should be well understood. There have been a large number of studies for high-field stress effects on thin oxide films, and significant progress has been made over the last two decades. However, most of the early researches on this subject have dealt with MOS capacitors and/or MOSFET's, and the degradation of the tunnel gate oxide of flash memories have been inferred based on the measurement results of the MOS devices. According to early studies, the oxide degradation is very sensitive to the fabrication process and device parameters, and the magnitude of the effects is found to depend strongly on the device fabrication details [4], [5]. Considering the significant fabrication differences between MOS devices and flash EEPROM's, it is uncertain whether the results from conventional MOS structures can properly predict the degradation of the tunnel oxide in flash EEPROM's. Moreover, there have not been many comprehensive models that can explain overall oxide degradation and breakdown mechanisms.

In this paper, we investigate the degradation of the tunnel gate oxide under FN tunneling stress by using a flash EEPROM structure. This can lead to a better understanding of the nature of oxide degradation in flash memory devices.

II. EXPERIMENTAL

The test devices (Fig. 1) used in this study are n-channel flash EEPROM's fabricated with a double-gate flash EEPROM device process. They were fabricated on (100) n-type Si substrates with 16–25 Ω·cm resistivity. A pocket p-well is formed by a 2.1×10^{13} cm^{-2}, 80-keV boron implant in the n-well with a 1.7×10^{13} cm^{-2}, 100-keV phosphorus implant. Gate oxides, approximately 100 and 200 Å thick, are grown as tunnel oxides. The n-type floating poly-Si gate was doped with $POCl_3$ with a sheet resistance of 365 Ω/sq. and 1500 Å thickness. The insulator films on the floating poly-Si gate were an ONO film (50 Å SiO_2 + 100 Å Si_3N_4 + 50 Å SiO_2). Then an n-type polycide control gate was formed by a conventional

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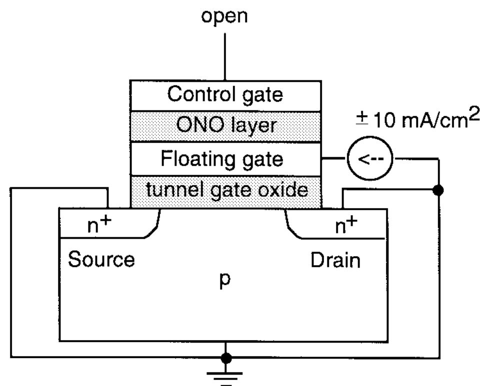


Fig. 1. Schematic cross section of a flash EEPROM and experimental setup for the current stress measurements.

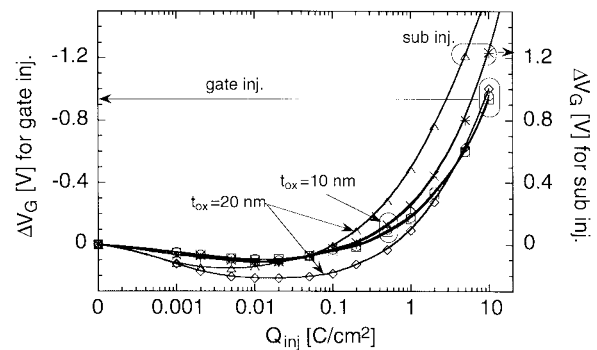


Fig. 2. Gate voltage shift ΔV_G versus injected charge density $Q_{\rm inj}$ for injection stress of both polarities. Initial values of V_G (before stress) for gate injection stress and substrate injection stress with $t_{\rm ox} = 100$ and 200 Å devices are about -11.307, -20.375, 10.376, and 19.048 V, respectively.

$POCl_3$ process with a sheet resistance of 55 Ω/sq. and a 1500 Å thick WSi was deposited by CVD. The n-type source/drain (S/D) implant (As, 50-keV, 5×10^{15} cm^{-2}) was performed after a gate etching process. The highest temperature for heat treatment after gate patterning was 970 °C. The final S/D diffusion junction depth was approximately 0.3 μm with a sheet resistance of 50–70 Ω/sq..

The devices in our experiments are flash EEPROM devices with an additional electrical contact to the floating gate. This allows us to emulate the real situation in flash EEPROM's where charge transfer occurs through the gate oxide between the floating gate and Si substrate. The devices have channel width (W)/channel length (L) ratios of 100/20 and 200/20 μm/μm for the 100 Å gate oxide, and 100/100 μm/μm for the 200 Å gate oxide. Constant current stress and I–V measurements were made with an HP4145B semiconductor parameter analyzer. In the stress measurements, MOSFET's were biased into either "substrate"- or "gate"-injection tunneling by applying positive or negative current to the floating gate. Both source and drain are grounded so that they can supply electrons for tunneling. A constant current density (J) of ± 10 mA/cm^2 was used for all constant current stress measurements. This current density is comparable to that encountered in EEPROM's and requires a 9–10 MV/cm electric field across the tunnel oxide film.

The I–V characteristics were first measured before any stress for an initial parameter check. The devices were then subjected to FN current stress using a constant current source. After known time intervals, the stress was interrupted and I–V plots were remeasured. This procedure was repeated until the devices broke down.

III. Results and Discussions

A. Gate Voltage, V_G

Under continuous constant FN current stress, charges are trapped in the oxide, necessitating a change in gate voltage V_G to maintain the constant current through the oxide. For example, negative charges (electrons) trapped in the oxide lower the magnitude of oxide field, consequently the magnitude of V_G should increase to retain a constant current flow. Likewise, the magnitude of V_G should decrease for positive charge (hole). Therefore, the gate voltage shift ΔV_G, defined as the change of gate voltage due to the stress compared to the pre-stress value, can provide the properties of the charges trapped in the oxide. Its sign depends on the direction of stress as well as the polarity of charge trapped in the oxide. Under substrate injection stress, ΔV_G is negative for hole trapping and positive for electron trapping. Similarly, under gate injection stress, ΔV_G is positive for hole trapping and negative for electron trapping.

The gate voltage shifts under F–N current stress are shown in Fig. 2. Here, $Q_{\rm inj}$ is the injected charge density obtained by multiplying the current density (J) by the stress time (t), $Q_{inj} = J \cdot t$. All ΔV_G curves go through either minimum or maximum values around 0.01 C/cm^2 and begin to turn around. The turnaround has been widely discussed in the literature [6]–[8]. The occurrence of the turnaround suggests that not only negative charges but also positive charges can be generated during the stress. Positive charges are dominantly generated in the oxide at low $Q_{\rm inj}$ followed by negative charges at high $Q_{\rm inj}$. The position and the mechanisms producing the positive oxide charges, responsible for the turnaround of ΔV_G, are still controversial. However, the generation of positive charges is generally attributed to either hole trapping [9], [10] or electron detrapping [7], [11], caused by impact ionization [12]. As the stress increases, the generation of negative charges in the oxide exceeds that of positive charges, causing ΔV_G to turn around. The generation of negative charges is mainly due to the trapping of electrons injected into the oxide during the constant current stress. Another observation is that once ΔV_G passes the turnaround, it keeps increasing with stress until breakdown occurs at about 5–15 C/cm^2. Since ΔV_G does not saturate, it is generally considered that both the generation of new electron traps as well as the electron trapping in existing traps contribute to the negative charges [7], [13]. After the turnaround, the change of ΔV_G becomes larger for substrate injection stress than gate injection stress, implying that substrate injection stress generates more negative charges or less positive charges in the oxide.

It is also observed that ΔV_G changes differently depending on the stress direction and oxide thickness. The change of ΔV_G is more evident for thick than for thin oxides throughout all stress periods. For thick (200 Å) oxide devices, the turnaround of ΔV_G is deeper and the overall change of ΔV_G is larger

than those of thin (100 Å) oxide devices. Gate injection stress creates a deeper turnaround at a higher $Q_{\rm inj}$ than does substrate injection stress. All the above observations suggest that the generation and trapping of both positive and negative oxide charges are enhanced for thicker oxide [14], and that the generation of positive charges increases under gate injection stress.

B. Threshold Voltage, V_T

The threshold voltage, V_T, is one of the most important parameters from a device operational point of view. For an n-channel enhancement mode MOSFET on uniformly doped substrates with no short- or narrow-channel effects, and with both source and substrate grounded, the threshold voltage can be expressed as

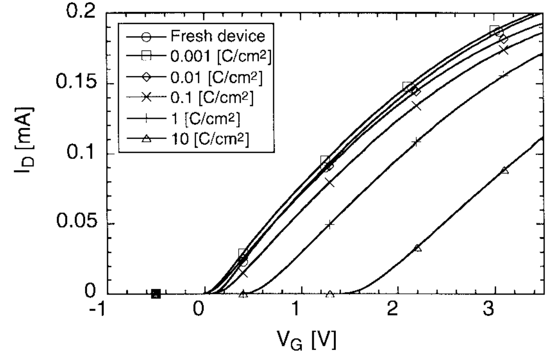
$$V_T = 2\phi_F + \frac{\sqrt{2qK_S\varepsilon_O N_A(2\phi_F)}}{C_{\rm ox}} + \phi_{MS} - \frac{\gamma Q_{\rm ox}}{C_{\rm ox}} - \frac{Q_{\rm it}(\phi_S = 2\phi_F)}{C_{\rm ox}} \quad (1)$$

where ϕ_F is the Fermi potential, q the electron charge, K_s the silicon dielectric constant, ε_o the permittivity of free space, N_A the acceptor doping concentration, $C_{\rm ox}$ the oxide capacitance, ϕ_{MS} the metal-semiconductor work function difference, and γ the charge distribution factor [15]. Here, $Q_{\rm ox}$ is defined as the trapped-oxide sheet charge density and $Q_{\rm it}$ the Si/SiO_2 interface charge density in C/cm^2. $Q_{\rm ox}$ includes all charge components that are not sensitive to silicon surface potential such as the trapped-oxide charge $Q_{\rm ot}$ and the fixed oxide charge Q_f. On the other hand, $Q_{\rm it}$ strongly depends on the silicon surface potential. The change in threshold voltage ΔV_T resulting from charge trapping in the oxide is then given as

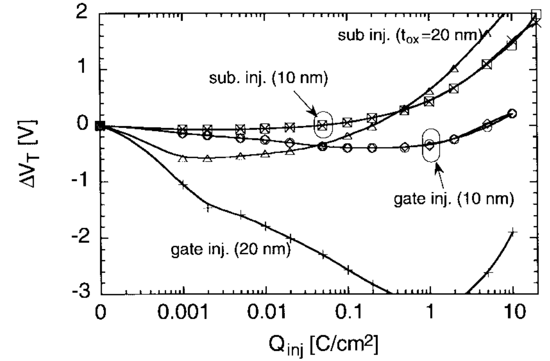
$$\Delta V_T = -\frac{\gamma\,\Delta Q_{\rm ox}}{C_{\rm ox}} - \frac{\Delta Q_{\rm it}(\phi_S = 2\phi_F)}{C_{\rm ox}}. \quad (2)$$

Equation (2) indicates that the threshold voltage shift takes into account the effect of both trapped-oxide charge and interface traps.

Typical I_D–V_G characteristics for n-MOSFET's under substrate injection stress are shown in Fig. 3(a). The effects of the stress appear as a shift in the I_D–V_G curve along the V_G axis and a decrease in the slope of the I_D–V_G curve. The threshold voltage shifts due to the stress are shown in Fig. 3(b). The overall trends of ΔV_T are similar to those of ΔV_G such as the formation of the turnaround and their polarity and oxide thickness dependence. The turnaround of ΔV_T is observed for all stress conditions, and the depth of the turnaround varies depending on the stress polarity and oxide thickness. At low $Q_{\rm inj}$, positive charge buildup in the oxide dominates, causing the threshold voltage to decrease. As stress increases, the generation and trapping of negative oxide charges prevail, and the threshold voltage shift turns around into the positive direction. The turnaround occurs at about the same $Q_{\rm inj}$ for each polarity stress, independent of the gate oxide thickness. Specifically, the turnaround points were observed around 0.5–1.0 and 0.002–0.005 C/cm^2 for gate injection and substrate injection stress, respectively.



(a)



(b)

Fig. 3. (a) I_D–V_G plots for n-MOSFET's ($V_D = 50$ mV) under substrate injection stress and (b) threshold voltage shift ΔV_T versus $Q_{\rm inj}$ for injection of both directions. Initial (unstressed) V_T are 0.14 and 0.23 V for $t_{\rm ox} = 100$ and 200 Å devices, respectively.

Gate injection stress differs from substrate injection stress in that the turnaround of ΔV_T appears deeper in the negative direction at a higher $Q_{\rm inj}$. Thick oxide creates a deeper turnaround for either polarity stress, which is consistent with the results of ΔV_G. A large deviation between ΔV_T and ΔV_G is noticed for gate injection stress, and the deviation becomes larger for thick oxides. This indicates that positive charge trapping mainly occurs near the Si/SiO_2 interface with its higher generation rate under the gate injection stress and for thicker oxides. All these observations suggest that gate injection stress involves more positive charge trapping near the Si/SiO_2 interface than does substrate injection. The positive charges are due to holes, either injected from the anode or created by an impact ionization process, and/or positive interface charges. Since the thick oxide is more susceptible to impact ionization, the positive charge buildup occurs even faster, and thus larger negative ΔV_T result for thick oxide devices. As electron injection through the oxide increases, electron trapping usually dominates over positive oxide charge trapping, and thus ΔV_T eventually increases in the positive direction. Under gate injection stress for a 200 Å oxide device, however, the effect of positive oxide charge trapping is large enough for ΔV_T to remain negative during the entire stress period.

C. Subthreshold Swing, S

A useful parameter in the subthreshold regime of I_D–V_G characteristics is the gate-voltage swing S. It is defined as the gate voltage required to change the current by one decade

[16]–[18], and is given by

$$S = 2.3\frac{kT}{q}\frac{1 + C_D/C_{\rm ox} + C_{\rm it}/C_{\rm ox}}{1 - (C_D/C_{FB})^2} \tag{3}$$

where C_D, $C_{\rm ox}$, $C_{\rm it}$, and C_{FB} are the depletion layer, the oxide, the interface trap, and the flat-band capacitances, respectively. $C_{\rm it} = qD_{\rm it}$, and $D_{\rm it}$ is interface trap density in $\text{cm}^{-2}\text{-eV}^{-1}$. Considering the generation of interface traps due to stress, the subthreshold swing change ΔS can be expressed as

$$\begin{aligned}\Delta S &= S(\text{after stress}) - S(\text{before stress}) \\ &= 2.3\frac{kT}{q}\frac{\Delta C_{\rm it}/C_{\rm ox}}{1 - (C_D/C_{FB})^2}\end{aligned}$$

where $\Delta C_{\rm it}$ is the interface trap capacitance change due to stress. Therefore, the change in interface trap density due to stress, $\Delta D_{\rm it}$, is directly related to ΔS as

$$\Delta D_{\rm it} = \frac{C_{\rm ox}\Delta S}{2.3kT}\left[1 - \left(\frac{C_D}{C_{FB}}\right)^2\right]. \tag{4}$$

Fig. 4(a) shows the subthreshold I_D–V_G characteristics under substrate injection stress. The subthreshold I_D–V_G curve shifts along the V_G axis and its slope is degraded with stress. This is an indication of both oxide charge trapping and Si/SiO_2 interface charge trapping. The degradation of the subthreshold current slope is mainly due to the generation of interface traps, and is shown in Fig. 4(b) as a function of stress. Subthreshold swing ΔS increases under both gate and substrate injection stress, and it keeps increasing with increasing stress. The degradation of subthreshold swing is more severe under gate injection stress, implying that gate injection stress creates more interface traps. In addition, thick oxides clearly experience more degradation of ΔS compared to thin oxides, suggesting that thick oxides are more sensitive to the interface trap generation due to stress.

On the other hand, as substrate injection stress increases, a severe distortion of the subthreshold I_D–V_G curve appeared, making the subthreshold slope difficult to interpret. It consists of an anomalous high leakage current component in the lower half of the distortion and normal subthreshold current behavior in the upper half. However, no clear distortion of I_D–V_G was observed under gate injection stress. The exact mechanism causing the distortion is not well known at this time, but it is likely related to the high leakage current underneath the field oxide between source and drain [19]. In normal n-MOSFET operation conditions, the thick field oxide as well as the p^+-channel-stop implant prevent the source-to-drain leakage along the edges of the silicon island. However, if an inversion layer can be formed under the field oxide prior to the inversion of the silicon surface under the gate oxide due to the degradation of the field oxide, the leakage current dominates the subthreshold current characteristics at low gate voltage values. Since the distortion of the subthreshold current curve appears under substrate injection stress only, it is considered that the field oxide degradation is much more serious under substrate injection than gate injection stress.

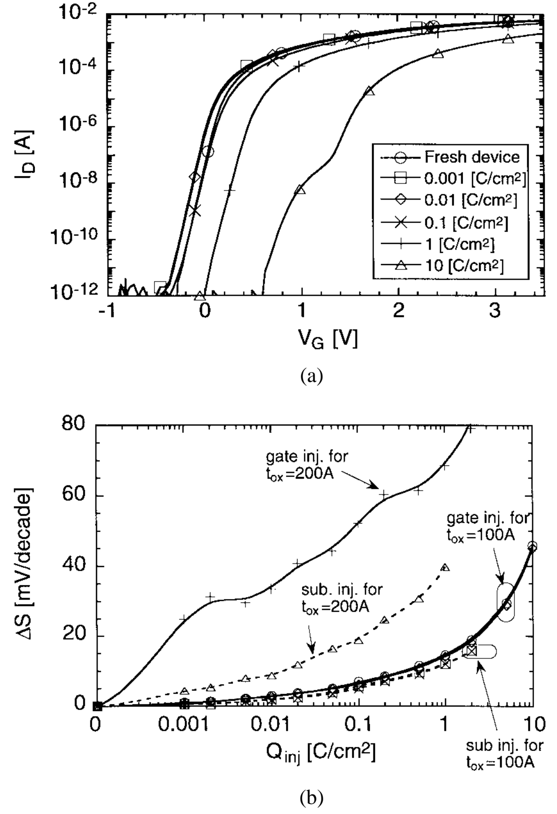


Fig. 4. (a) Subthreshold current versus gate voltage characteristics ($V_D = 2$ V) under substrate injection stress and (b) the extracted subthreshold swing change ΔS for injection of both directions. Initial S (before stress) values of n-MOSFET's with $t_{\rm ox} = 100$ and 200 Å are about 67 and 74 mV/decade, respectively.

D. Trapped-Oxide Charge Voltage Shift ($\Delta V_{\rm ot}$) and Interface Trap Voltage Shift ($\Delta V_{\rm it}$)

The threshold voltage shift under high-field stress reflects the generation of both interface traps and trapped-oxide charge, i.e., $\Delta V_T = \Delta V_{\rm it} + \Delta V_{\rm ot}$, where $\Delta V_{\rm it}$ and $\Delta V_{\rm ot}$ are the voltage shifts due to interface traps and trapped-oxide charge, respectively. It is often that ΔV_T alone cannot provide enough information on oxide degradation due to stress, and the separation of ΔV_T into $\Delta V_{\rm it}$ and $\Delta V_{\rm ot}$ needs to be done [20]. It is based on the general assumption that interface traps in the upper half of the band gap are acceptors and those in the lower half of the band gap are donors, having interface traps uncharged at the midgap condition ($\phi_s = \phi_F$). First, the midgap current ($I_{\rm mg}$), defined as the current at the midgap condition, is obtained from the subthreshold current equation [21]

$$\begin{aligned}I_D = &\mu_{\rm eff}\left(\frac{W}{L}\right)\frac{aC_{\rm ox}}{2\beta^2}\left(\frac{n_i}{N_A}\right)^2 \\ &\cdot (1 - e^{-\beta V_D})e^{-\beta\phi_S}(\beta\phi_S)^{-1/2}\end{aligned} \tag{5}$$

where $\mu_{\rm eff}$ is the effective electron mobility, $\beta = q/kT$, and n_i the intrinsic carrier concentration. With the midgap current, the corresponding midgap voltage shift ($\Delta V_{\rm mg}$) can be monitored with stress, and this represents the shift due to trapped charge in the oxide only, i.e., $\Delta V_{\rm mg} = \Delta V_{\rm ot}$. Since the midgap current generally is very small (less than 1 pA), the

subthreshold curve must be linearly extrapolated to the current level to locate the midgap voltage. The shift in the threshold voltage due to interface traps is then the difference between the midgap and threshold voltage shifts and is given by

$$\Delta V_{\rm it} = \Delta V_T - \Delta V_{\rm mg}.$$

Once $\Delta V_{\rm mg}$ and $\Delta V_{\rm it}$ are known, the density of trapped-oxide charge and interface traps can be determined by $\Delta N_{\rm ot} = \Delta V_{\rm mg} C_{\rm ox}/q$ and $\Delta N_{\rm it} = \Delta V_{\rm it} C_{\rm ox}/q$, respectively. Here, $\Delta N_{\rm it}$ represents the density of interface traps between midgap and threshold conditions.

Fig. 5(a) shows typical ΔV_T, $\Delta V_{\rm mg}$, and $\Delta V_{\rm it}$ under gate injection stress. The midgap voltage shift is slightly less than the threshold voltage shift, but both show similar trends with stress. The voltage shift due to interface traps $\Delta V_{\rm it}$ increases in the positive direction with stress, indicating an increase of interface traps. This also supports the assumption that the upper half of the band gap are acceptors because the acceptor interface traps are negatively charged between midgap and threshold conditions, resulting in a positive voltage shift. Fig. 5(b) and (c) present $\Delta N_{\rm ot}$ and $\Delta N_{\rm it}$ under gate and substrate injection stress. Again, the turnaround of $\Delta N_{\rm ot}$ is indicative of dominant positive oxide charge trapping at low $Q_{\rm inj}$ followed by dominant negative oxide charge trapping at high $Q_{\rm inj}$. Interface trap density keeps increasing with increasing stress, which is consistent with the subthreshold slope data. It is evident that gate injection stress creates more positive oxide charges and interface traps than does substrate injection stress. Positive oxide charge trapping is higher for thicker oxide under either stress direction.

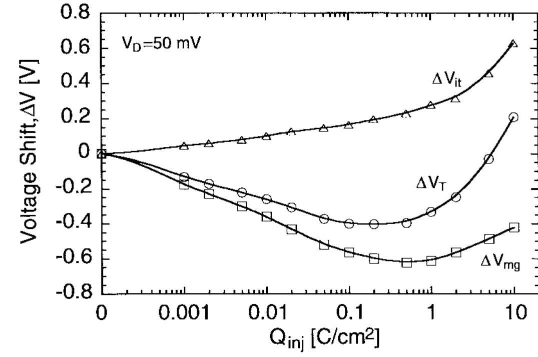
E. Transconductance, g_m

Another important parameter that characterizes a MOSFET is the transconductance, g_m. In the linear region, it is defined as

$$g_m = \frac{\partial I_D}{\partial V_G} = \mu_{\rm eff} C_{\rm ox} \frac{W}{L} V_D, \text{ for } V_D < V_{D,sat} \quad (6)$$

where $V_{D,sat}$ is the saturation drain voltage. It is apparent from (6) that g_m is proportional to $\mu_{\rm eff}$. Since $\mu_{\rm eff}$ depends on lattice and Coulomb scattering by oxide and interface charges, one of the direct consequences of stress is the reduction of the transconductance [22], [23].

The g_m versus V_G curves obtained from I_D–V_G curves under substrate injection stress are shown in Fig. 6(a). Clearly, the transconductance is degraded as well as shifted along the V_G axis as a result of stress. The transconductance curve shift is mainly due to charge trapping in the oxide, and agrees with the threshold voltage shift. On the other hand, the reduction of transconductance reflects the reduced channel mobility due to the charge trapping in the oxide and at the Si/SiO_2 interface. The degradation of maximum transconductance is shown in Fig. 6(b) as a function of stress. The $g_{m,\max}$ degradation under gate injection stress turned out to be more serious than that under substrate injection stress, which is consistent with the results of ΔS and $\Delta N_{\rm it}$. The $g_{m,\max}$ degradation rate is relatively constant for each stress polarity independent of oxide thickness and gate area, and it is always higher under



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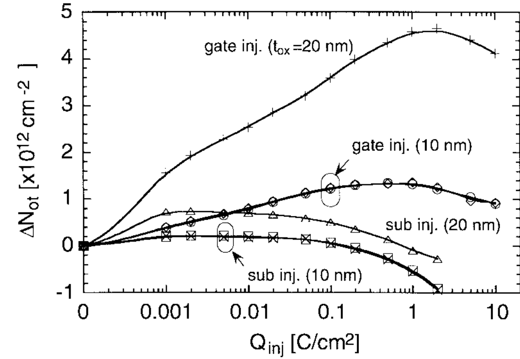

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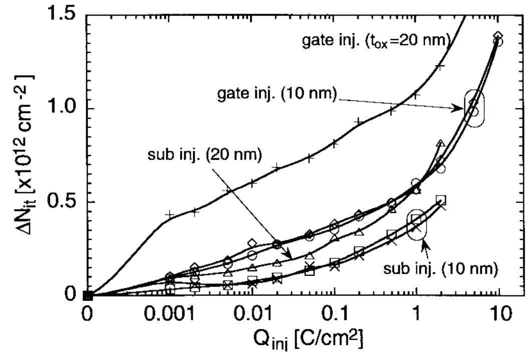

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Fig. 5. (a) Typical threshold voltage shift and its separation into voltage shifts due to trapped-oxide charge and interface traps under gate injection stress, $W = 200$ μm, $L = 20$ μm, $t_{\rm ox} = 100$ Å, (b) change of trapped-oxide charge density, and (c) interface trap density under stress.

gate injection stress than substrate injection stress. Specifically, at 10 C/cm^2 of $Q_{\rm inj}$, the $g_{m,\max}$ of gate and substrate injection stress drops about 50 and 30% compared with the unstressed conditions, respectively.

F. Charge-to-Breakdown, $Q_{\rm bd}$

As charge is transported through the oxide a wear-out phenomenon occurs, even at very low currents. Once the total charge transported through the oxide accumulates a "charge-to-breakdown" level, $Q_{\rm bd}$, a short-circuit between the gate and the silicon substrate develops. Since $Q_{\rm bd}$ depends on oxide and interfacial quality, it has been widely used as a measure of reliability, and it is determined by the

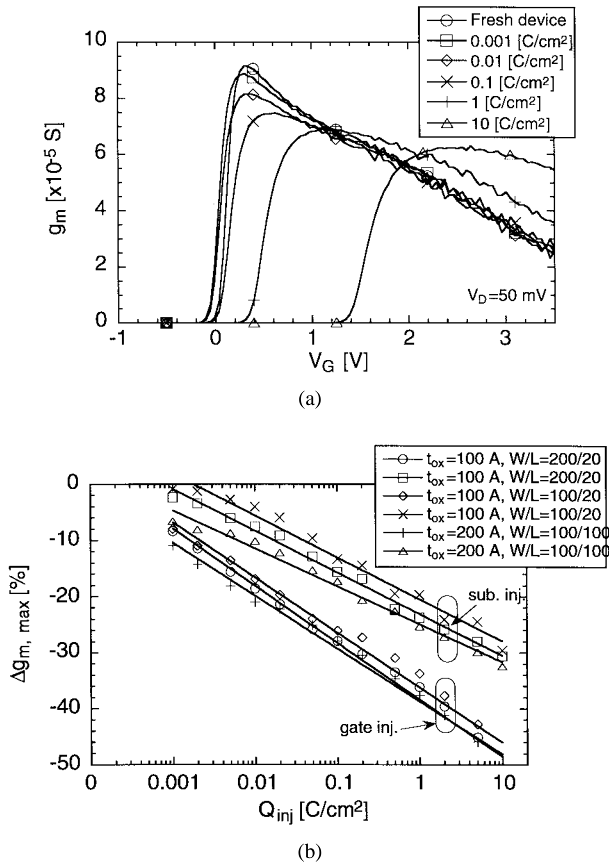

Fig. 6. (a) Transconductance versus gate voltage characteristics under substrate injection stress and (b) the maximum transconductance shift $\Delta g_{m,\max}$. Initial $g_{m,\max}$ (before stress) values of n-MOSFET's with $t_{\rm ox} = 100$ Å ($W/L = 200/20$), 100 Å ($W/L = 100/20$) and 200 Å ($W/L = 100/100$) are about 8.8×10^{-5}, 4.3×10^{-5}, and 5×10^{-6} S, respectively.

time-dependent-dielectric-breakdown (TDDB) technique using constant-current stress. Breakdown is conventionally defined as a sudden drop in the voltage magnitude needed to maintain a constant current. Constant-current stress ensures that the stress conditions such as the electric field at the injecting electrode and the F–N current are fixed. Hence, a clear connection between a specific stress condition and the resultant breakdown characteristics can be established. It is also a convenient way to characterize the integrity of the gate oxide. This type of stress roughly emulates the conditions experienced in nonvolatile EEPROM memories, which rely on the tunneling of electrons to and from a floating gate.

Fig. 7 shows $Q_{\rm bd}$ of n-MOSFET's for injection of both polarities. Here, $Q_{\rm bd}$ was obtained by multiplying the current density (J) by the time-to-breakdown ($t_{\rm bd}$), $Q_{\rm bd} = J \cdot t_{\rm bd}$. Although there exists experimental scatter in the $Q_{\rm bd}$ data, the general trend is that $Q_{\rm bd}$ of substrate injection stress is higher than that of gate injection stress. This agrees with previous reports [24]–[26], and suggests either that more significant damage in the oxide occurs under gate injection stress than substrate injection stress and/or that the poly-Si/SiO_2 interface is weaker than the Si/SiO_2 interface mainly due to the rougher poly-Si/SiO_2 interface. The $Q_{\rm bd}$ of thick oxides, with larger scatter in data, is relatively lower than that of thin oxides, implying that thicker oxides are weaker under high-field stress.

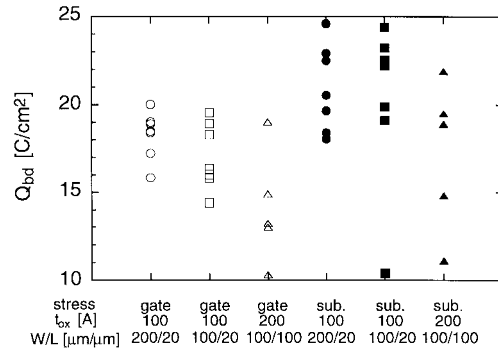

Fig. 7. Charge-to-breakdown under F–N constant current stress.

IV. Breakdown Model

The oxide breakdown model is based on all the experimental results and analyzes. Our high-field stress data show serious oxide degradation phenomena under stress in the form of electron and hole generation and their trapping in the oxide, and trap generation in the oxide and at the Si/SiO_2 interface. All of them degrade oxide quality in one way or another and result in oxide breakdown.

We believe that physical damage to the oxide plays a key role. The source of such damage is the energetic electrons flowing through the oxide from the cathode to the anode. Under constant current stress, as shown in Fig. 8, electrons tunnel through a triangular barrier via the F–N tunneling mechanism, then travel through the conduction band of the oxide while undergoing scattering events. Some electrons get trapped at existing and newly created traps, which produces a net negative charge throughout the stress period. If the kinetic energy (KE) of electrons in the applied field is sufficient for impact ionization, electron-hole pairs and new traps are generated, hence contributing additional negative and positive charges. The impact ionization process [12] has a strong dependence on oxide thickness and electric field. It can be band gap or trap ionization depending on the magnitude of KE that the electrons gain. Band gap ionization occurs when the electrons have energy greater than 9 eV. Since the average kinetic energy gained by the electrons in the oxide conduction band increases with increasing electric field, band gap ionization is enhanced under higher field. The KE gained in a given field also depends on the distance traveled in the oxide conduction band. If the distance is not sufficient, the KE of an average electron can not build up to a band gap ionization threshold, and impact ionization is less likely to take place. Thus thick oxides have more electrons with energies greater than the impact ionization threshold compared to thin oxides. The band gap ionization also occurs at the anode interface. When they are discharged at the anode, the electrons release both the KE gained in the field, and the potential energy (PE), the energy difference between the bottom of the oxide conduction band and the anode conduction band. If this energy release at the anode is greater than the impact ionization threshold (~3.2 eV), it can cause physical damage in the form of band gap ionization, trap generation, or bond breaking. On the other hand, trap ionization is considered when the mean kinetic energy of electrons in the oxide is about 4–5 eV,

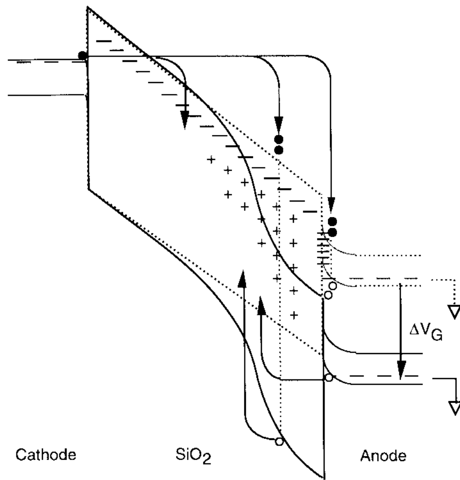

Fig. 8. Schematic band diagram of an MOS structure before (dotted line) and after (solid line) charge generation due to F–N current injection. Electrons are injected from the cathode, and get trapped as they move to the anode. Some electrons attain sufficient KE for impact ionization in the oxide and at the anode. Also shown is the possible hole injection from the anode due to the increased anode electric field after stress.

which is well below the threshold for band gap. This energy, however, is sufficient to detrap electrons in defect states within the SiO_2 band gap by impact ionization, and it can generate negative and positive bulk charges by electron trapping and detrapping.

Once holes are generated under impact ionization, they are relatively immobile and tend to be caught in trap sites near their points of origin. Hence, more positive charge trapping appears in the oxide closer to the anode, causing V_T shift in the negative direction. Trap generation occurs at the interfaces as well as in the oxide, but interface trap generation at the anode is particularly severe due to the large amount of energy imparted by the electrons to weak interfacial bonds. As a result of charge trapping and trap generation, the electric field in the oxide is no longer uniform but increases locally. This accelerates impact ionization, contributing more damage in the oxide. At breakdown, all the damage sites in the oxide link, and a conductive path between cathode and anode is formed.

The stress direction dependence of the observed device characteristics can be understood with this model. For gate injection stress, holes are trapped near the Si substrate, and interface traps are generated at the Si/SiO_2 interface, i.e., heavier damage at the Si/SiO_2 (anode) interface. As a result, they affect device characteristics like V_T, S, and g_m. Similarly, for substrate injection stress, holes are trapped near the poly-Si gate and interface traps are generated at the poly-Si/SiO_2 interface, causing more damage at the poly-Si/SiO_2 (anode) interface. However, they do not affect the device characteristics as much as for gate injection stress because their location is far away from the Si/SiO_2 interface. The dependence of $Q_{\rm bd}$ on the stress direction appears to be involved with the interface roughness. For gate injection stress, the heavier damage in the oxide near the anode (Si/SiO_2) links up with the rougher cathode (poly-Si/SiO_2) interface. Therefore, oxide breakdown under gate injection stress is reached earlier than under substrate injection stress, where the heavier damage near the anode (poly-Si/SiO_2) connects to the smoother cathode (Si/SiO_2) interface. The dependence of $Q_{\rm bd}$ on the oxide thickness is also evident by considering the impact ionization process. Since the thicker oxides are more susceptible to impact ionization, the physical damage occurs faster for thicker oxide, and thus lower $Q_{\rm bd}$ results.

V. Discussion and Conclusion

In this study we have presented the effects of high-field stress on oxide degradation. Our main interest was on the stress-induced oxide degradation of "flash EEPROM" devices. In these devices, the operation involves electrons flowing through a thin tunnel gate oxide between the Si substrate and a floating poly-Si gate under a high electric field across the gate oxide. Therefore, problems related with charge flow through the oxide under high electric field are critical issues for flash memories. We employed flash EEPROM test structures and emulated the real situation in flash EEPROM's by applying a high electric field on the tunnel gate oxide between the floating gate and Si substrate. This provided us better understanding of the tunnel gate oxide degradation in the flash memory devices. Under F–N high-field stress, several types of damage occurred in the tunnel gate oxide of flash EEPROM devices. This damage, in the form of positive and negative charge formation in the oxide as well as the generation of interface states at both the poly-Si/SiO_2 and the Si/SiO_2 interfaces, degrades the overall device performance and shortens its operating lifetime.

We observed a turnaround of ΔV_G and ΔV_T under constant F–N stress. The occurrence of the turnaround is an indication that positive charge trapping in the oxide is dominant at low $Q_{\rm inj}$, followed by negative charge trapping at high $Q_{\rm inj}$. The nonsaturating behavior of V_G implies that oxide traps are not merely filled with negative charges, but are created continuously until breakdown occurs. ΔV_G depends on oxide thickness as well as stress direction. For thicker oxides, a deeper turnaround of ΔV_G is formed due to more positive charge trapping in the oxide. The turnaround of ΔV_G is deeper under gate injection stress than substrate injection stress. The positive charge is mainly due to holes created by an impact ionization process, which is enhanced for thick oxides and seems more active under gate injection stress, evidenced by results of $\Delta N_{\rm ot}$. The threshold voltage shift ΔV_T follows the same trend as ΔV_G, but the magnitude of the change is different with respect to each other. The difference reflects that positive charge trapping takes place near the Si/SiO_2 interface, causing large ΔV_T in the negative direction.

The effect of high-field stress on the generation of interface traps has been investigated by monitoring the change of g_m, the subthreshold current, and the subthreshold current slope. The interface trap density increases with increasing $Q_{\rm inj}$, and its increase is accelerated for thick oxides. The generation of interface states at the Si/SiO_2 interface is higher under gate injection than substrate injection, implying that stress induced damage at the Si/SiO_2 interface is heavier under gate injection stress. However, the damage in the field oxide seems more serious under substrate injection stress, evidenced by severe distortion of the subthreshold I_D–V_G curve. In addition, a very

clear distinction between gate injection and substrate injection is observed from $\Delta g_{m,\max}$. The degradation rate of $g_{m,\max}$ under gate injection stress is always higher than that under substrate injection stress.

Charge-to-breakdown $Q_{\rm bd}$ of MOSFET's also shows stress direction and thickness dependence. Oxide breakdown is accelerated under gate injection stress and more severe damage in the oxide results for thicker oxides. Large scatter of $Q_{\rm bd}$ data indicates that $Q_{\rm bd}$ may be affected by poly-Si/SiO_2 and Si/SiO_2 surface roughness as well.

By combining all results, a simple model of oxide degradation and breakdown was constructed. According to the model, the oxide damage appears more serious near and at the anode interface by impact ionization, and oxide breakdown is closely related to the surface roughness of both interfaces. When all the damage sites in the oxide can link up with each other and a conductive path between cathode and anode is formed, oxide breakdown occurs. If the cathode interface is rough or weak, this makes it easier for a conductive leakage path between the cathode and anode to form because the anode is heavily damaged by the stress. The damage is more serious for thicker oxides because the thicker oxides are more susceptible to impact ionization. Hole trapping, in particular, dominantly takes place near the anode interface. Holes, generated by impact ionization, are relatively immobile and tend to be caught in trap sites near their points of origin (anode). Hence, more positive charge trapping appears in the oxide closer to the anode, causing higher ΔV_T in the negative direction. Interface traps are also created predominantly at the anode interface, degrading both g_m and S.

Therefore, the model also suggests that having a smoother surface at both Si/SiO_2 and poly-Si/SiO_2 interfaces as well as thinner oxides can improve both oxide degradation and breakdown under high-field stress.

REFERENCES

[1] J. Eldridge, "Flash memory goes mainstream," *IEEE Spectrum,* vol. 30, pp. 48–54, Oct. 1993.

[2] S. Aritome, R. Shirota, G. Hemink, T. Endoh, and F. Masuoka, "Reliability issues of flash memory cells," *Proc. IEEE,* vol. 81, pp. 776–787, May 1993.

[3] G. Verma and N. Mielke, "Reliability performance of ETOX based flash memories," in *Proc. IRPS,* 1988, pp. 158–166.

[4] D. Crook, M. Domnitei, M. Webb, and J. Bonini, "Evaluation of modern gate oxide technologies to process charging," in *Proc. IRPS,* 1993, pp. 255–261.

[5] H. Miki, M. Noguchi, K. Yokogawa, B.-W. Kim, K. Asada, and T. Sugano, "Electron and hole traps in SiO_2 films thermally grown on Si substrates in ultra-dry oxygen," *IEEE Trans. Electron Devices,* vol. ED-35, pp. 2245–2252, Dec. 1988.

[6] M. Itsumi, "Positive and negative charging of thermally grown SiO_2 induced by Fowler–Nordheim emission," *J. Appl. Phys.,* vol. 52, pp. 3491–3497, May 1981.

[7] M. P. Fazan, M. Dutoit, C. Martin, and M. Ilegems, "Charge generation in thin SiO_2 polysilicon-gate MOS capacitors," *Solid State Electron.,* vol. 30, pp. 829–834, Aug. 1987.

[8] S. K. Lai and D. R. Young, "Effects of avalanche injection of electrons into silicon dioxide-generation of fast and slow interface states," *J. Appl. Phys.,* vol. 52, pp. 6231–6240, Oct. 1981.

[9] S. Holland, I. C. Chen, T. P. Ma, and C. Hu, "On physical models for gate oxide breakdown," *IEEE Electron Device Lett.,* vol. EDL-5, pp. 302–305, Aug. 1984.

[10] I. C. Chen, S. E. Holland, and C. Hu, "Electrical breakdown in thin gate and tunneling oxides," *IEEE Trans. Electron Devices,* vol. ED-32, pp. 413–422, Feb. 1985.

[11] Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky, "Dynamic model of trapping-detrapping in SiO_2," *J. Appl. Phys.,* vol. 58, pp. 2252–2261, Sept. 1985.

[12] D. J. DiMaria, T. N. Theis, J. R. Kirtley, F. L. Pesavento, and D. W. Dong, "Electron heating in silicon dioxide and off-stoichiometric silicon dioxide films," *J. Appl. Phys.,* vol. 57, pp. 1214–1238, Feb. 1985.

[13] E. Harari, "Dielectric breakdown in electrically stressed thin films of thermal SiO_2," *J. Appl. Phys.,* vol. 49, pp. 2478–2489, Apr. 1978.

[14] D. J. DiMaria, E. Cartier, and D. Arnold, "Impact ionization, trap creation, degradation, and breakdown in silicon dioxide films on silicon," *J. Appl. Phys.,* vol. 73, pp. 3367–3384, Apr. 1993.

[15] D. K. Schroder, *Semiconductor Material and Device Characterization.* New York: Wiley, 1990, p. 253.

[16] J. R. Brews, "Subthreshold behavior of uniformly and nonuniformly doped long-channel MOSFET," *IEEE Trans. Electron Devices,* vol. ED-26, pp. 1282–1291, Sept. 1979.

[17] S. Horiguchi, T. Kobayashi, and K. Saito, "Interface-trap generation modeling of Fowler–Nordheim tunnel injection into ultra-thin gate oxide," *J. Appl. Phys.,* vol. 58, pp. 387–391, July 1985.

[18] C. Tan, M. Xu, and Y. Wang, "Application of the difference subthreshold swing analysis to study generation interface trap in MOS structures due to Fowler–Nordheim aging," *IEEE Electron Device Lett.,* vol. 15, pp. 257–259, July 1994.

[19] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI.* Boston, MA: Kluwer, 1991, pp. 94–98.

[20] P. J. McWhorter and P. S. Winokur, "Simple technique for separating the effects of interface traps and trapped-oxide charge in metal-oxide-semiconductor transistors," *Appl. Phys. Lett.,* vol. 48, pp. 133–135, Jan. 1986.

[21] S. M. Sze, *Physics of Semiconductor Devices.* New York: Wiley, 1990, pp. 446–448.

[22] M.-S. Liang, C. Chang, Y. T. Yeow, C. Hu, and R. W. Brodersen, "MOSFET degradation due to stressing of thin oxide," *IEEE Trans. Electron. Devices,* vol. ED-31, pp. 1238–1244, Sept. 1984.

[23] M. S. Liang, S. Haddad, W. Cox, and S. Cagnina, "Degradation of very thin gate oxide MOS devices under dynamic high field/current stress," in *IEDM Tech. Dig.,* 1986, pp. 394–398.

[24] P. P. Apte, T. Kubata, and K. C. Saraswat, "Constant current stress breakdown in ultrathin SiO_2 films," *J. Electrochem. Soc.,* vol. 140, pp. 770–773, Mar. 1993.

[25] S. S. Gong, M. E. Burnham, N. D. Theodore, and D. K. Schroder, "Evaluation of $Q_{\rm bd}$ for electrons tunneling from the Si/SiO_2 interface compared to electron tunneling from the poly-Si/SiO_2 interface," *IEEE Trans. Electron Devices,* vol. 40, pp. 1251–1257, July 1993.

[26] K. Naruke, S. Taguchi, and M. Wada, "Stress induced leakage current limiting to scale down EEPROM tunnel oxide thickness," in *IEDM Tech Dig.,* 1988, pp. 424–427.

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