Low-Frequency Noise in TFSOI Lateral N-P-N Bipolar Transistors

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***Abstract*—Low-frequency $(1/f)$ noise is characterized as a function of base current density (J_B) on thin-film-silicon-on-insulator (TFSOI) lateral bipolar transistors [1]. In the low injection region of operation, the noise power spectral density was proportional to $J_B^{1.8}$ for $J_B < 0.4$ μA/μm^2, which suggest that the noise in these devices is primarily dominated by a uniform distribution of noise sources across the emitter-base area. However in the high current region of operation $(J_B > 0.4\ \mu\text{A}/\mu\text{m}^2)$, the noise bias dependence shifts to $J_B^{1.2}$ indicating current crowding effects alter the contribution of noise sources near the extrinsic base link region of the device. In addition to the expected $1/f$ noise and shot noise, we have observed a bias dependent generation-recombination (G/R) noise source in some of the devices. This G/R noise is correlated to random-telegraph-signal (RTS) noise resulting from single trapping centers, located at or near the spacer oxide and/or the Si to SIMOX interface, which modulate the emitter-base space charge region.**

***Index Terms*—Flicker noise, generation-recombination (GR) noise, lateral bipolar junction transistor (BJT), npn, 1/f noise, random-telegraph-signal (RTS) noise, SOI, TFSOI BiCMOS, thin-film silicon-on-insulator.**

I. Introduction

As THE demands for low-power, low-voltage, and high-speed VLSI circuits increase, TFSOI technology has recently emerged as a viable choice for many low-power RFIC mixed-mode applications. These technologies which are capable of operating at low power supply voltages will become paramount to the development and success of the next generation of low cost commercial products such as mobile communications systems, cellular phones, pagers, PCs, etc. [2]–[9]. Recent developments in bonding wafer techniques and **S**eparation-by-**IM**planted-**OX**ygen (SIMOX) and increasing demand for higher performance integrated circuits (ICs) has led to higher quality, lower cost, and more widely available SOI starting material [10]–[14]. When compared to bulk silicon for 1.0 V applications, SOI provides superior device performance with potential for substantial reductions in die cost that can be achieved through reduced process complexity and increased device layout densities [2], [15]–[20]. Several key advantages of TFSOI BiCMOS include reduced parasitic capacitance, reduced crosstalk effects, near-ideal subthreshold characteristics, enhanced mobility, latchup immunity, low voltage compatibility, high current drive, high temperature performance, ESD tolerance, and capability for high-speed high reliability applications [1], [21]–[26].

While TFSOI shows exceptional promise for low-voltage radio-frequency (RF) and microwave applications [27]–[40], only minor details of the low frequency noise properties of lateral BJTs on TFSOI, where the emitter-base junction rests on the Si buried oxide, have been reported [41]. Transistor low-frequency $(1/f)$ noise is a key design constraint [42], [43] and important figure-of-merit in rf and analog circuits, because it places a fundamental limit on the achievable spectral purity of a system [44]–[47]. For example, intrinsic low-frequency noise can be up-converted in rf mixers, oscillators, and power amplifiers due to nonlinearity in the devices [48]–[53]. This spurious up-converted noise appears as noise sidebands centered around the rf carrier signal in the output spectrum and can thus place serious limitations on the overall performance of a system [44], [54]–[58]. In this paper, we present the first investigation of the low frequency noise properties of TFSOI bipolar transistors as a function of bias and emitter area geometry. We also demonstrate the $1/f$ noise characteristics of TFSOI BJTs are best described by a number fluctuations model in the low-injection region of operation while current crowding effects dominate in the high-current region of operation.

II. Device Technology and Experimental Setup

Bipolar transistors were fabricated using a TFSOI CBiCMOS process which has been described in detail by Huang *et al.*, [1]. In brief, the process uses SIMOX substrate material with a nominal silicon thickness of 1000 Å and buried oxide thickness of 4000 Å. The technology is based on a fully manufacturable process developed for 0.5 μm LDD CMOS and lateral bipolar devices. Platinum silicide base poly-Si contacts are used to enhance high-frequency performance through reduced base resistance and minimized current crowding effects. poly-buffered-LOCOS oxide isolates both bipolar and MOS devices. Integration is completed with two layers of metallization. Fig. 1 shows a schematic cross-section of the TFSOI lateral n-p-n bipolar transistor. A SEM cross-section of the completed bipolar transistor with a self-aligned silicide is shown in Fig. 2.

Low-frequency noise measurements were made with the transistor biased in the high source resistance, common emitter configuration using a HP 3561A Dynamic Signal Analyzer.

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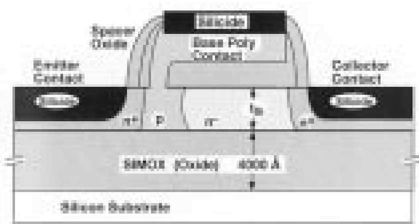

Fig. 1. General schematic cross-section of a TFSOI lateral n-p-n bipolar transistor.

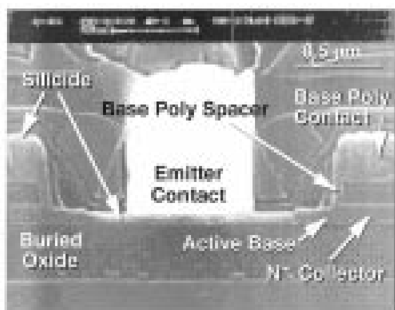

Fig. 2. SEM cross-section of the completed TFSOI lateral bipolar transistor with a self-aligned silicide [1].

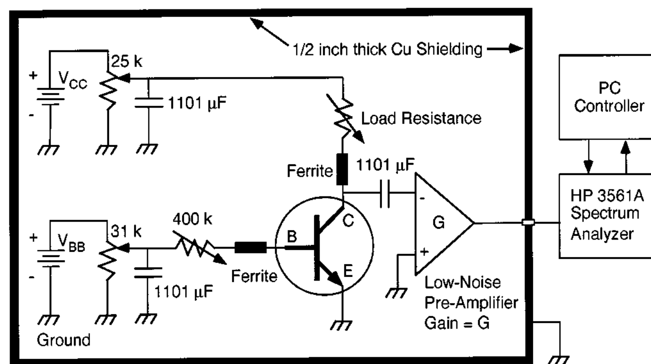

Fig. 3. Schematic of the $1/f$ noise measurement setup.

The general schematic of the measurement setup is shown in Fig. 3. A 1/2–in thick copper shielded box achieved excellent isolation of the device under test from extraneous outside noise sources. Wire wound bias resistors and battery supply voltage sources minimized the bias network noise. High frequency ferrite chokes were used in order to achieve transistor stability without influence on the low frequency noise properties of the devices. Noise signal amplification was provided by a battery operated EG&G Low Noise Amplifier model 113 that was placed inside the shielded copper box. Pre- and post-noise electrical characteristics of the devices were measured using a HP 4145B Parameter Analyzer. An in-house specialized computer program controlled equipment interface and calculated the input-equivalent base-current-noise source (S_{IB}). The factor (A) representing magnitude of the low-frequency noise, $S_{IB} = A/f^{\lambda}$, was calculated by first converting the noise to a logarithmic scale and then using a general linear least squares fit [59] to obtain the intercept (A) and slope (λ) in the frequency range of 1.0 Hz to 10.0 Hz.

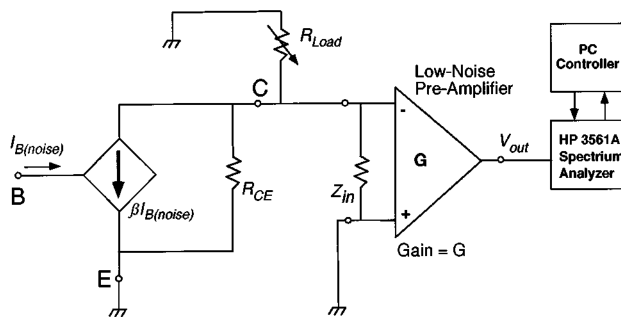

Fig. 4. Common emitter small signal circuit model used for calculating input referred noise from the measured output noise.

The noise measurement system integrity was verified by measuring theoretical shot noise in BJTs and by measuring several different wire wound resistors at various dc bias conditions with the measured result always equaling the calculated theoretical thermal noise.

III. Experimental Results

A. Fundamental $1/f$ Noise

In its most general form, low-frequency noise in a bipolar transistor is dominated by base flicker noise according to [60]:

$$S_{HRs} = S_{ifb} + S_{ifc}\big/\beta^2 + 2qI_B \tag{1}$$

where

- S_{HRs} measured input referred noise current spectral density;
- S_{ifb} base current noise source;
- S_{ifc} collector current noise source;
- $2qI_B$ shot noise of the device.

The units of the noise sources are in A^2/Hz. For the case of the common emitter configuration and high base resistance bias condition, it can be shown that the base current noise source dominates [61]–[72].

Fig. 4 shows the simplified small signal circuit model used for calculating input-referred noise for the common emitter configuration which uses a high base resistance bias condition. Note, in this simplified small signal circuit model we consider only the most dominant noise source due to the base noise spectra (S_{IB}), ignoring the noise contribution due to the collector noise spectra and the resistive elements in the bias circuits and preamplifier. Based on a small signal analysis, we can calculate the input referred base current noise power spectral density in units of A^2/Hz as,

$$S_{IB} = S_{VO}\Big/(G\beta R_{EQUIV})^2 \tag{2}$$

where

- S_{VO} measured voltage output noise at the spectrum analyzer;
- G gain of the pre-amplifier;
- β current gain of the BJT.

R_{EQUIV} is the parallel resistance combination of the load resistor R_L, the parasitic small signal shunt resistance (R_{CE}) between the collector and emitter of the BJT, and the input impedance (Z_{in}) of the pre-amplifier.

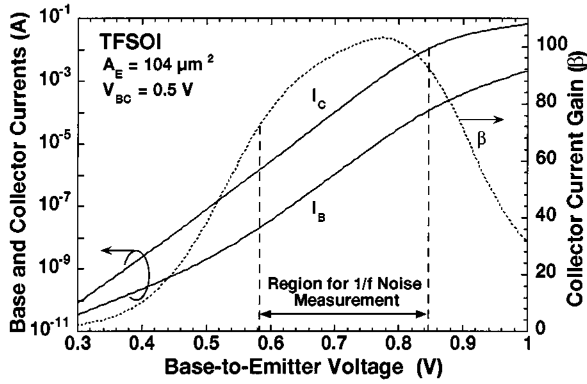

Fig. 5. Gummel and collector current gain (β) characteristic of a TFSOI BJT with emitter area (A_E) of $0.1 \times 7.2 \times 144 \approx 104$ $\mu\mathrm{m}^2$. Also shown, is the region over which low-frequency $(1/f)$ noise was measured ($I_B = 20$ nA to $I_B = 100$ μA).

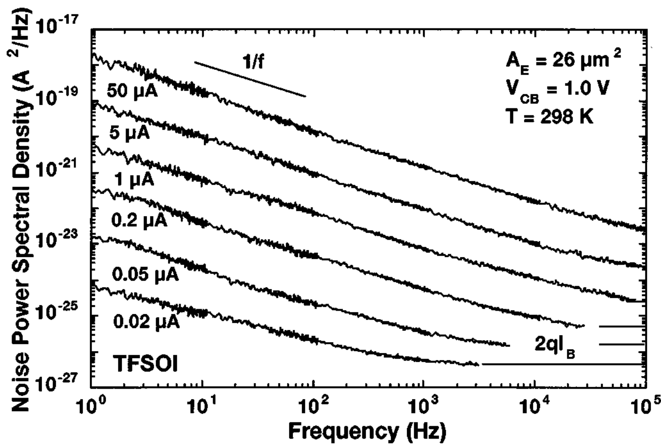

Fig. 6. Equivalent input referred base current noise power spectral density (S_{IB}) measured for a TFSOI BJT with $A_E = 0.1 \times 7.2 \times 36 \approx 26$ $\mu\mathrm{m}^2$. Starting from the bottom $1/f$ noise curve and increasing toward the top $1/f$ noise curve, $I_B = 20$ nA, 50 nA, 96 nA, 200 nA, 502 nA, 1.00 μA, 2.00 μA, 5.00 μA, 10.0 μA, 21.7 μA, and 52.2 μA.

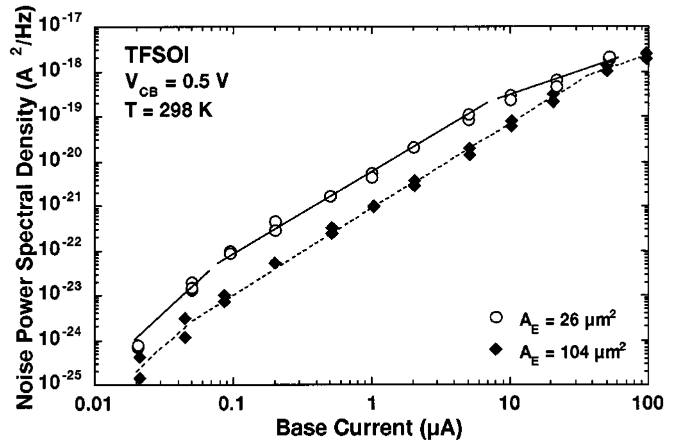

Fig. 7. Magnitude of the measured input-referred base current noise power spectrum at 1.0 Hz for a small area ($A_E = 26$ $\mu\mathrm{m}^2$) and large area device ($A_E = 104$ $\mu\mathrm{m}^2$) as a function of base current.

The typical Gummel characteristics and current gain (β) for a TFSOI lateral bipolar transistor with an emitter area (A_E) of 0.1 μm thickness $\times 7.2$ μm emitter width $\times 144$ fingers ≈ 104 $\mu\mathrm{m}^2$ is shown in Fig. 5. Also shown for clarity is the region in which $1/f$ noise measurements were made ($I_B = 20$ nA to $I_B = 100$ μA).

Fig. 6 shows the equivalent input-referred base current noise power spectral density (S_{IB}) measured as a function of base current for a TFSOI lateral BJT with $A_E = 26$ $\mu\mathrm{m}^2$. The noise spectra of this device exhibits a $1/f^\lambda$ behavior with $\lambda \approx 1.0$ at low frequencies and the magnitude of the $1/f$ noise increases monotonically with increasing base current. For this particular device, the slope λ varied between 0.84 to 1.11 for all measured data indicating a near ideal $1/f$ noise spectrum for all base bias conditions (20 nA to 52 μA). The base current bias dependence of the $1/f$ noise can be seen in Fig. 7, which shows the measured S_{IB} at 1.0 Hz for a small area device ($A_E = 26$ $\mu\mathrm{m}^2$) and a larger area device ($A_E = 104$ $\mu\mathrm{m}^2$) versus I_B. Both the large and small area devices show flicker noise described by three different dependencies in base current ($S_{IB} \sim I_B^k$). In the large area device, the $1/f$ noise is described by $k = 1.9$ for currents measured between 50 nA $< I_B <$ 32 μA. At high currents ($I_B >$ 32 μA), the large area device shows a linear power dependence with $k = 0.96$, while in the low current range ($I_B <$ 50 nA) $k \approx 2.7$. Similarly in the small area device, the $1/f$ noise has a base current power dependence of $k = 2.7$ in the low current range ($I_B <$ 50 nA), a power dependence of $k = 1.76$ in the intermediate current range (50 nA $< I_B <$ 10 μA), and $k = 1.25$ in the high current range ($I_B >$ 8 μA). These values are in agreement with those typically reported for base current flicker noise in BJTs, which show $1.0 < k < 3.0$ [73]–[75]. The roll-off observed in $1/f$ noise $(k \sim 3.0)$ at low base current may potentially be attributed to the base-emitter resistance ($r_\pi = \Delta V_{BE}/\Delta I_B$) approaching the value of the external base bias resistance of 400 kΩ used in this experiment [76]. However, the shift in bias dependence of the noise at very low base currents for the different size devices can not be completely explained by the bias resistance approaching r_π, since this value is only dependent on the bias current and not on the device geometry. Hence, these results indicate that there is a unique shift in the current dependence of the noise at low base current and at base resistance values near r_π. This shift in noise dependence, which is dependent on device geometry, is thus expected to be related to the interaction of the collector current noise source and the base current noise source."

Following the analysis in [61] and [77], the physical location of the noise source distribution can be determined by investigating the area and current dependence of the noise as determined from $S_{IB} = I_B^k A_E^{1-k}$. If $k = 2.0$, the noise sources are considered to be distributed uniformly across the emitter area (A_E). On the other hand if $k = 1.0$ and there is no area dependence on the measured noise, then the low-frequency noise is dominated by a mobility fluctuations model due to the diffusion of carriers across the base of the transistors [78]. Since diffusion is always present in a BJT operating in the forward active region, the fundamental limit on low-frequency noise in a BJT is governed by mobility fluctuations due to diffusion [79], [80] and white noise limitations. As the base current density increases, $1/f$ noise becomes dominated by a number fluctuations model if trapping centers exist [81]. Referring to Fig. 7, it is clear that these TFSOI bipolar transistors are dominated by noise sources

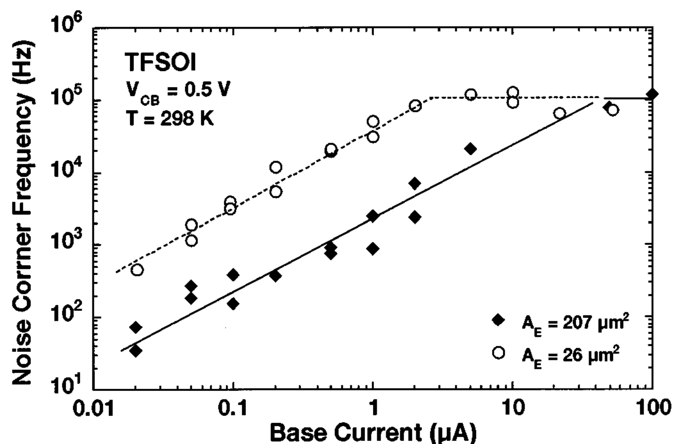

Fig. 8. Noise corner frequency (f_{CR}) versus base current for large and small area devices.

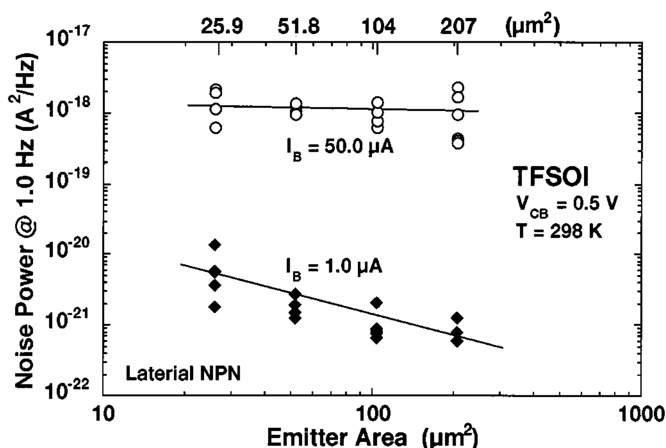

Fig. 9. Data showing the input referred base current noise power spectral density magnitude versus emitter area. Bottom curve shows S_{IB} measured at 1.0 μA, while the top curve shows S_{IB} measured at $I_B = 50$ μA.

which are distributed uniformly in space across the emitter area with $k \approx 2.0$ in the mid current range (100 nA $< I_B < 10$ μA). However, when these devices are in the high current density region of operation the noise becomes dominated by current crowding effects [82]. Based on the shift in noise dependence $(k \approx 1.0)$ at high current densities, we can infer that the noise sources in these devices are either 1) not uniformly contributing across the emitter area to the total noise generated at the output of the device or 2) current crowding begins to induce a decrease in the noise and in base resistance [83], such that the noise shifts to a linear dependence on base current.

Additional evidence for a shift in the noise mechanisms of these devices at high current densities can be seen in Fig. 8, which shows the measured corner frequency (f_{CR}) versus the base current. In Fig. 8, we have defined the corner frequency as the frequency for which the $1/f$ noise component is equal to the shot noise component. From these data points it is apparent that both the larger and small area devices show a linear I_B dependence of the corner frequency for most bias conditions. On the other hand, in the high current density regime f_{CR} becomes bias independent.

In Fig. 9, we plot the noise power spectral density measured at 1.0 Hz versus the emitter area for a base current of 1.0 μA (low-injection region) and a base current of 50.0 μA (high-current region). For low injection, one can observe that within the scatter of the data the $1/f$ noise is inversely proportional to the area of the device. By applying a least squares curve fit, the noise in this region of operation is proportional to $1/A_E^{0.92}$ with a unity area (1.0 μm^2) intercept of 8.2×10^{-20} A^2/Hz. The shift in noise source dependence in the high current region is again evidenced in the upper curve of Fig. 9, showing the input referred noise power versus emitter area at a constant base current of 50 μA for a fixed frequency (1.0 Hz). It is clear that in the high current region the noise in the devices has shifted from an inverse linear dependence on emitter area to one that is proportional to $1/A_E^{0.24}$.

Based on these observations, we conclude that $1/f$ noise in the low current region of operation is governed by a number fluctuations model uniformly distributed across the emitter area and not at the emitter periphery of the device [77]. Whereas in the high current region of operation, S_{IB} becomes dominated by current crowding effects that have modified the physical contributions or distribution of noise sources in the BJT toward the extrinsic base link region [82]–[84]. These results are consistent with simulation results showing that higher current densities occur near the extrinsic base link region [38]. These effects are expected to become more pronounced as the current crowding effects increase.

In view of the fact that the noise varies with both base current and emitter area $(S_{IB} = I_B^k A_E^{1-k})$, it is not apparent where the crossover point occurs for current crowding effects when measuring devices with different emitter areas. On the other hand, if we define the flicker noise in terms of the base current density (J_B) the noise dependence becomes readily apparent. As derived in [61], [85], the base current density noise power is given by $S_{JB} = J_b^k = S_{IB}/A_E$. Fig. 10 shows S_{JB} measured at 1.0 Hz versus base current density for TFSOI lateral BJTs investigated in this study. Within the scatter of the data in Fig. 10, the $1/f$ noise of a lateral TFSOI *npn* can be modeled by $J_B^{1.82}$ $(k = 1.82)$ bias dependence for $J_B < 0.4$ μA/μm^2 and $J_B^{1.2}$ $(k = 1.2)$ for $J_B > 0.4$ μA/μm^2.

Based on the current and area dependence of flicker noise in the BJTs described above, it can be difficult to compare $1/f$ noise produced by different BJT technologies without doing some type of normalization. A convenient and simple method for comparing $1/f$ noise in different devices and technologies is to multiply S_{IB} by the emitter area of the device $(S_{IB} \times A_E)$, assuming the noise is dominated by a square law dependence in the base current [67], [86], [87]. Within the scatter of the data in Fig. 10, the $1/f$ noise of a lateral TFSOI n-p-n can be modeled by a $I_B^{1.82}$ bias dependence and a normalized noise magnitude factor of $AF = 9.2 \times 10^{-9}$ μm^2 for $J_B < 0.4$ μA/μm^2. This noise level is similar to bulk silicon BJTs which utilize a conventional ion-implanted double polysilicon structure and have a normalized magnitude factor AF in the range of 4×10^{-9} μm^2 to 2×10^{-8} μm^2 [61], [86]–[89]. It is also similar to the noise found in the BJTs of a 0.5 μm high performance (15 GHz) mixed-signal polysilicon BiCMOS process that has AF factors in the range 4×10^{-9} μm^2 to 4×10^{-8} μm^2 [71]. Al-

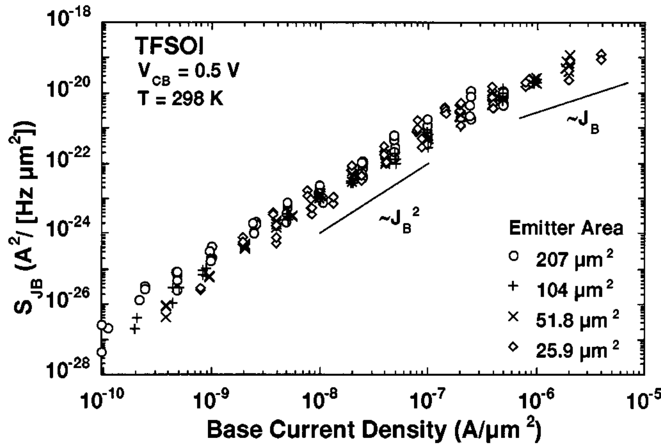

Fig. 10. Area normalized noise magnitude ($S_{JB} = S_{IB}/A_E$) versus base current density. Data in this figure represents 11 different devices obtained from two different wafer lots for the TFSOI technology.

though this noise level in the TFSOI technology may limit some ultralow noise circuit applications, the noise performance of these devices still far exceeds most MOS transistors and by far most GaAs devices [90], [91], which have AF in the range of 9×10^{-8} μm^2 to 1×10^{-7} μm^2 [92], [93].

B. G/R Noise and RTS Noise

Until this point, we have been primarily concerned with transistors dominated by "pure" $1/f$ noise and the theoretical shot noise. However it is not uncommon to find devices that show generation-recombination (G/R) noise in addition to the expected $1/f$ and shot noise components normally present [67], [68], [88], [89], [94]–[109]. We now introduce a modified low-frequency noise model [110] which describes the noise characteristics of a BJT under different bias conditions and for transistors with traps located at or near the emitter-base (EB) space-charge-region (SCR) as given by

$$S_{IB} = \frac{AF \times I_B^{KF}}{(Area)^{KF-1} f^{\lambda}} + \frac{B\tau(V_{BE}) \times I_B^2}{1 + (\omega\tau(V_{BE}))^2} + 2qI_B \quad (3)$$

where $\omega = 2\pi f$. The first term in (3) represents a slight modification of the SPICE $1/f$ noise model [111] by including λ (the frequency exponent dependence) and area dependence as given by Markus and Kleinpenning [61]. The second term represents the G/R noise due to traps located in the EB SCR with a time constant (τ) that are a function of the base-to-emitter bias (V_{BE}). This G/R noise is square law dependent on the base current [112], [113].

Because G/R noise was not observed in all devices we speculate the primary cause of the G/R noise to be single trapping centers located at or near the EB SCR. Indeed this turned out to be the case. Fig. 11 shows the correlated RTS noise produced in a device that displayed G/R noise. The abrupt shifts in RTS noise are a clear signature of single G/R trapping centers modulating the EB SCR. This is significant since it shows that single G/R centers located in the EB SCR will have a substantial influence on the low-frequency noise. It also provides a basic technique to characterize the defect density for a particular BJT technology.

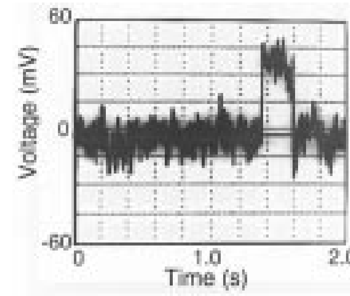

Fig. 11. TFSOI device showing random-telegraph-signal (RTS) noise.

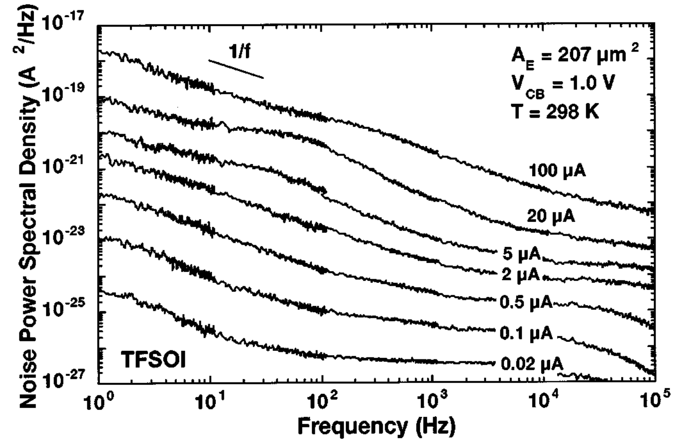

Fig. 12. TFSOI BJT showing the appearance and then virtual disappearance of generation-recombination (G/R) noise, seen as a Lorentzian shaped hump superimposed on the $1/f$ noise, measured at different base currents. Starting from the bottom $1/f$ noise curve and increasing toward the top $1/f$ noise curve, I_B = 20 nA, 50 nA, 100 nA, 200 nA, 501 nA, 1.00 μA, 2.00 μA, 5.00 μA, 9.94 μA, 19.8 μA, 49.7 μA, and 101 μA.

Fig. 12 shows the observed appearance and then virtual disappearance of G/R noise, seen as a "Lorentzian shaped hump" superimposed on the $1/f$ noise, for different base currents [94]. Below 5.0 μA, the TFSOI BJT shows almost pure $1/f$ noise characteristics in the low-frequency range followed by the expected theoretical shot noise in the high frequency range. However, for this particular device, we observe the sudden appearance of a Lorentzian shaped hump at a base current of about 5.0 μA. The time constant τ associated with G/R noise can be found by taking $1/2\pi f_{GR} = 3.5$ ms, where f_{GR} is the 3-dB break frequency associated with the G/R noise (45 Hz in this case). When the base current reaches approximately 100 μA the G/R noise virtually disappears, suggesting that the higher base bias condition has moved the emitter-base space-charge-region away from the G/R trapping centers, eliminating their modulation of the G/R noise [67].

The disappearance of G/R noise in the device shown in Fig. 12 for I_B below 5.0 μA remains unexplained at this point. However, these results may suggest that this G/R noise trapping-center in this device is located where current crowding causes the G/R noise to be enhanced in this device. It is speculated that at the lower bias current the G/R center becomes less effective in modulating the base and collector currents, possibly due to a more uniform current conduction in the base region of the device. At higher currents, the current crowding [38], [114] may force the current conduction closer to the G/R trapping-center

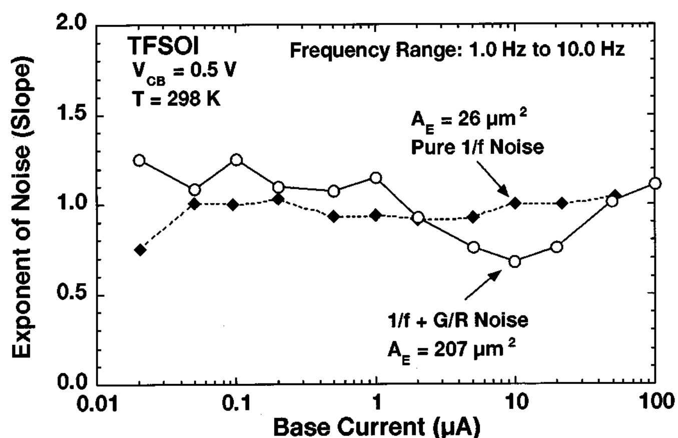

Fig. 13. Effect of base current bias on the exponent factor (slope λ) of the noise for a device showing $1/f$ noise and for a device showing both $1/f$ noise and G/R noise. Note, the slope λ was obtained by doing a least squares fit on the noise data measured in the frequency range from 1.0 to 10 Hz, which included 400 data points with 60 time averages each.

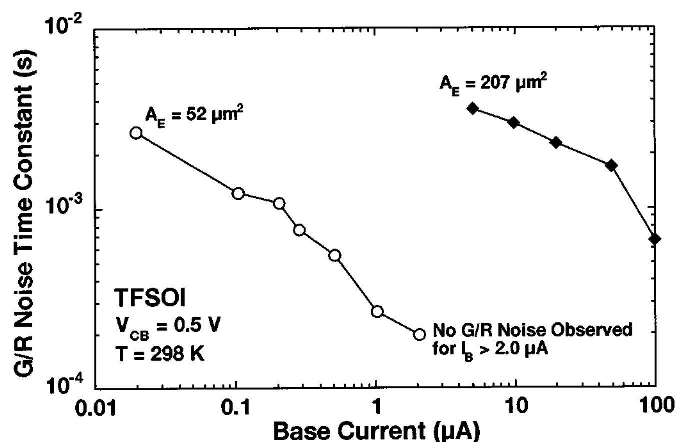

Fig. 14. Data displaying the base current bias dependence of the G/R noise time constant (τ_{GR}) for two different TFSOI BJTs. Note, for the smaller sized BJT ($A_E = 52\ \mu\text{m}^2$), no G/R noise was observed for base currents above 2.0 μA which suggests the higher V_{BE} bias has shifted the G/R centers outside of the emitter-base space-charge-region.

and hence the trap can modulate the base and collector current through fluctuations in the space charge potential in this region as evidenced by the appearance of random telegraph signal noise which was correlated with this G/R noise. At very high currents, the space charge region (SCR) collapses and the G/R center moves outside the SCR and thus can no longer cause G/R noise. One possible location for this G/R trap is in the base polysilicon-to-single crystal silicon interface separating the extrinsic base region from the intrinsic base region of the device. Current crowding will cause a higher percentage of emitter/collector current to flow near this region and hence may be the reason for the observed G/R noise dependence.

The effect of base current on the exponent of the noise (slope λ) for a small and large area BJT is shown in Fig. 13. For the small area device, the exponent λ is virtually 1.0 with deviation only occurring at the lowest I_B. While the large size device shows λ to initially be close to 1.0, then as the time constant of the G/R noise moves into the frequency range used to calculate λ (1.0 Hz to 10.0 Hz), the slope shifts to values less then 1.0. The slope λ reaches a minimum ($I_B = 10\ \mu$A) when the trap modulating the G/R noise is centered in the frequency range between 1.0 and 10 Hz. At higher bias conditions, the G/R center moves out of the frequency range and the slope λ increases to unity or near ideal $1/f$ noise. These results are similar to those reported by Scholz *et al.*, [115], except in their case the authors used a change in temperature to shift the time constant of the G/R noise instead of bias condition. The effects of bias on the G/R noise time constant ($\tau_{GR} = 1/2\pi f_{GR}$) are shown in Fig. 14 for two different sized BJTs. It is evident from these data that the time constant associated with the G/R noise (τ_{GR}) monotonically decreases with increasing I_B.

We believe there are two equally plausible explanations for the observed τ_{GR} dependence on EB bias. For the first model, it is suggested that the potential well associated with the G/R noise has been modified by the emitter-base bias condition [116]. This effect can be visualized by referring to Fig. 15, which shows an illustration of how the presence of a trapping center in the EB SCR may appear under a forward active base bias condition.

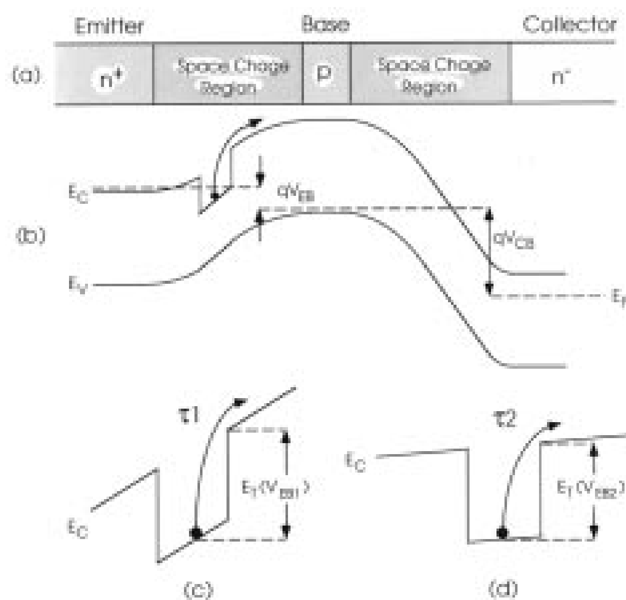

Fig. 15. Schematic band diagram representation of a n-p-n BJT with a trapping center located in the emitter-base space-charge-region (SCR) that can modulate the G/R noise of the transistor. (a) Shows a basic n-p-n cross-section. (b) Energy band diagram representing a forward active biased n-p-n transistor with a trapping center located in the EB SCR. (c) The potential well of the trapping center under an applied bias of V_{EB1}, where $\tau 1$ is the time constant of the trap. (d) The case where $V_{EB2} > V_{EB1}$, under this condition we have $ET(V_{EB2}) < ET(V_{EB1})$ which results in $\tau 2 < \tau 1$.

Note, this is not a steady state diagram, but instead represents the actual conditions under which the $1/f$ noise was measured. In Fig. 15(c) and (d), we illustrate the effects of low V_{BE} bias versus high V_{BE} bias on the potential well and the probability or time constant τ_{GR} associated with the emission or capture of a carrier. Based on the direction of current flow in a forward active biased n-p-n BJT and by momentum conservation arguments, we can assume in this model that the electron will have a higher probability of being emitted from the trap to the base region of the device and not to the emitter region of the device.

Under these conditions, it is clear that the time constant associated with the G/R noise will decrease as V_{BE} increases due to the lowering of the potential barrier (E_T) at higher V_{BE}. Once the trap is located outside the EB SCR, it can no longer modulate the EB SCR and thus the G/R noise disappears as was observed in Fig. 13 for the device with an emitter area of 52 μm^2.

For the second model, we assume an enhancement in the probability of carrier emission from the trap through impact ionization [117]. In this case hot carriers injected from the emitter to the base can transfer some of their energy to a trapped electron causing its subsequent emission from the trap. As V_{BE} increases, the electrons emitted from the emitter-to-base will have a slightly higher energy with respect to the trap and a proportionally larger number of electrons will be available for stimulating emission from the trap. Under these assumptions, we can obtain a decrease in τ_{GR} as V_{BE} increases. Modulation of the G/R noise will be affected via these processes so long as the trap remains inside or within a Debye length of the EB space charge region. When the forward bias potential forces the trap outside of the EB space charge region, carrier capture and emission by the trap can no longer modulate the EB space charge region, thus eliminating the G/R noise that is observed at lower bias conditions.

IV. Discussion and Summary

TFSOI lateral n-p-n BJTs show fundamental $1/f$ noise in the low-frequency range, followed by the theoretically expected shot noise in the higher frequency range. In the low current density region of operation $(J_B < 0.4\ \mu A/\mu m^2)$, we observed a noise dependence $S_{JB} \sim J_B^{1.83}$, which suggests a uniform distribution of noise sources across the emitter area. However, in the high current density region of operation $(J_B > 0.4\ \mu A/\mu m^2)$, the noise power spectral density was proportional to $J_B^{1.25}$, which suggests current crowding effects cause either 1) the noise sources to nonuniformly contribute across the emitter area to the total noise generated or 2) current crowding induces a decrease in the noise and in base resistance [83], such that the noise shifts to a linear dependence on base current.

Because of the unique structure of these lateral TFSOI BJT's (i.e., no polysilicon-to-emitter contact is used), we conclude that the $1/f$ noise source in these devices has two possible origins. 1) Carrier number fluctuations model dominated by traps in the spacer oxide or SIMOX oxide at the boundary of the emitter-base space charge region [80]; 2) Fluctuations in the barrier height between the single-crystal-silicon-to-polysilicon base contact of these devices.

A small portion of the devices measured showed G/R noise superimposed on the $1/f$ and shot noise of the transistor. This G/R noise was correlated to RTS noise and is indicative of single G/R trapping centers modulating the EB SCR and we have revealed that the emitter-base bias can shift the time constant associated with this noise. We observe the probability of finding G/R noise increases in proportion to the emitter area, which indicates G/R noise is correlated to the defect density affecting the EB SCR in TFSOI BJTs.

Finally, we have shown that the $1/f$ noise in these TFSOI BJTs is comparable to high performance bulk silicon self-aligned polysilicon-emitter BJT's that use conventional ion implant techniques for the base doping profile. Although the $1/f$ noise level encountered in these TFSOI BJTs may impose some limitations for ultra-low-noise-amplifiers (LNA), they still far exceed the noise performance of most MOS transistors and GaAs devices. Secondly, by modifying process conditions [71], [109], [118]–[127] or improved quality SIMOX starting material, we believe it should be possible for TFSOI technology to approach the noise performance of the best bulk silicon devices while maintaining advantages for high-frequency low voltage IC applications.

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References

[1] W.-L. M. Huang *et al.*, "TFSOI complementary BiCMOS technology for low power applications," *IEEE Trans. Electron Devices*, vol. 42, pp. 506–512, Mar. 1995.

[2] P. K. Vasudev, M. Mendicino, and T. E. Seidel, "Advanced materials for low power electronics," *Solid-State Electron.*, vol. 39, no. 4, pp. 489–497, 1996.

[3] R. H. Reuss *et al.*, "Trends in devices for low power," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1994, pp. 19–22.

[4] S. Urabe and T. Nojima, "Developments in mobile/portable telephones and key devices for miniaturization," *IEICE Trans. Electron.*, vol. E79-C, pp. 600–605, 1996.

[5] Z. J. Lemnios, "Silicon-on-insulator technology for low power electronics," in *Proc. 1995 URSI Int. Symp. Signals, Syst. Electron. (ISSSE)*, 1995, pp. 271–274.

[6] J. D. Meindl, "Low power microelectronics: Retrospect and prospect," *Proc. IEEE*, vol. 83, pp. 619–635, 1995.

[7] J. M. C. Stork, "Technology leverage for ultra-low power information systems," *Proc. IEEE*, vol. 83, pp. 607–618, 1995.

[8] S. Malhi and P. Chatterjee, "1-V microsystems 'Scaling on schedule for personal communications'," *IEEE Circuits Devices*, vol. 10, pp. 13–17, Mar. 1994.

[9] G. Yeap and A. Wild, "Introduction to low-power VLSI design," *Int. J. High Speed Electron. Syst.*, vol. 7, pp. 223–248, 1996.

[10] A. J. Auberton-Hervé *et al.*, "SOI materials for ULSI applications," *Semicond. Int.*, pp. 97–104, Oct. 1995.

[11] M. Alles and W. Krull, "Advanced manufacturing of SIMOX for low power electronics," *Solid-State Electron.*, vol. 39, pp. 499–504, 1996.

[12] S. R. Wilson *et al.*, "Materials, device and gate oxide integrity evaluation of SIMOX and bonded SOI wafers," in *Proc. IEEE Int. SOI Conf.*, 1995, pp. 143–145.

[13] H. J. Hovel, "Silicon-on-insulator substrates: Status and prognosis," in *Proc. IEEE SOI Conf.*, 1996, pp. 1–3.

[14] J. Seo, J. C. Woo, M. Mendicino, and P. K. Vasudev, "Charge-to-breakdown of thin gate oxide and buried oxide on SIMOX SOI wafers," *J. Electrochem. Soc.*, vol. 144, pp. 499–504, 1997.

[15] P. K. Vasudev, "CMOS devices and interconnect technology enhancements for low power/low voltage applications," *Solid-State Electron.*, vol. 39, no. 4, pp. 481–487, 1996.

[16] W.-L. M. Huang *et al.*, "TFSOI BiCMOS technology for low power applications," in *IEDM Tech. Dig.*, 1994, pp. 449–452.

[17] B.-Y. Hwang *et al.*, "SOI for low-power applications," in *Ext. Abst. Int. Conf. Solid State Devices Mater.*, 1994, pp. 268–270.

[18] B.-Y. Hwang *et al.*, "Design and manufacturing considerations of a 0.5 μm CMOS technology on TFSOI," in *IEEE Int. SOI Conf. Proc.*, 1993, pp. 128–129.

[19] A. J. Auberton-Hervé, "SOI: Materials to system," in *IEDM Tech. Dig.*, 1996, pp. 3–8.
[20] B. El-Kareh, B. Chen, and T. Stanley, "Silicon on insulator—An emerging high-leverage technology," *IEEE Trans. Components, Packaging Manuf. Technol. A*, vol. 18, pp. 187–194, 1995.
[21] J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Boston, MA: Kluwer, 1991.
[22] Y. Zhang, "Modeling of SOI MOSFET's for low power integrated circuits," Ph.D. Dissertation, Arizona State Univ., Tempe, 1997.
[23] P. Francis, A. Terao, B. Gentinne, D. Flandre, and J.-P. Colinge, "SOI technology for high-temperature applications," in *IEDM Tech. Dig.*, 1992, pp. 353–356.
[24] J.-P. Raskin, A. Viviani, D. Flandre, and J.-P. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Trans. Electron Devices*, vol. 44, pp. 2252–2261, Dec. 1997.
[25] S. H. Voldman, "The impact of technology evolution and scaling on electrostatic discharge (ESD) protection in high-pin count high-performance microprocessors," in *IEEE ISSCC Dig.*, 1999, pp. 366–367.
[26] G. G. Shahidi *et al.*, "Device and circuit design issues in SOI technology," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1999, pp. 339–346.
[27] J. P. Colinge, "Recent advances in SOI technology," in *IEDM Tech. Dig.*, 1994, pp. 817–820.
[28] M. H. Hanes *et al.*, "MICROX™—An all-silicon technology for monolithic microwave integrated circuits," *IEEE Electron Device Lett.*, vol. 14, pp. 219–221, May 1993.
[29] N. Camilleri, D. Lovelace, J. Costa, and D. Ngo, "New development trends for silicon RF device technologies," in *IEEE Microwave Millimeter-Wave Monolithic Circuits Symp. Dig.*, 1994, pp. 5–8.
[30] W. M. Huang *et al.*, "TFSOI complementary BiCMOS technology for low power RF mixed-mode applications," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1996, pp. 35–38.
[31] G. G. Shahidi *et al.*, "A novel high-performance lateral bipolar on SOI," in *IEDM Tech. Dig.*, 1991, pp. 663–666.
[32] R. Dekker, W. T. A. Einden, and H. G. R. Maas, "An ultra low power lateral bipolar polysilicon emitter technology on SOI," in *IEDM Tech. Dig.*, 1993, pp. 75–78.
[33] D. Hisamoto *et al.*, "Silicon RF devices fabricated by ULSI processes featuring 0.1-μm SOI-CMOS and suspended inductors," in *Symp. VLSI Tech. Dig.*, 1996, pp. 104–105.
[34] R. Dekker *et al.*, "An ultra low power RF bipolar technology on glass," in *IEDM Tech. Dig.*, 1997, pp. 921–923.
[35] T. Tanaka, Y. Momiyama, and T. Sugii, "Fmax enhancement of dynamic threshold-voltage MOSFET (DTMOS) under ultra-low supply voltage," in *IEDM Tech. Dig.*, 1997, pp. 423–426.
[36] W. M. Huang *et al.*, "TFSOI technology for portable wireless communications systems," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1997, pp. 421–426.
[37] V. M. C. Chen and J. C. S. Woo, "A low thermal budget, fully self-aligned lateral BJT thin film SOI substrate for low power BiCMOS applications," in *Symp. VLSI Tech. Dig.*, 1995, pp. 133–134.
[38] S. Kawanaka *et al.*, "3-D simulation analysis of high performance SOI lateral BJT for RF applications," in *Proc. IEEE Int. SOI Conf.*, 1998, pp. 29–30.
[39] T. Shino *et al.*, "A 31 GHz $f_{\max}$ lateral BJT on SOI using self-aligned external base formation technology," in *IEDM Tech. Dig.*, 1998, pp. 953–956.
[40] H. Nii *et al.*, "A 67 GHz $f_{\max}$ lateral bipolar transistor with co-silicided base electrode structure on thin film SOI for RF analog applications," in *Proc. ESSDREC*, 1999, pp. 212–215.
[41] J. A. Babcock, W. M. Huang, J. M. Ford, D. Ngo, D. J. Spooner, and S. Cheng, "Low-frequency noise dependence of TFSOI BiCMOS for low power RF mixed mode applications," in *IEDM Tech. Dig.*, 1996, pp. 133–136.
[42] R. P. Jindal, "Low-frequency fluctuations device, technology, and system implications," in *Quantum 1/f Noise and Other Low Frequency Fluctuations in Electronic Devices*, P. H. Handel and A. L. Chung, Eds. New York: AIP, 1993, vol. AIP Conf. Proc. 282, pp. 1–7.
[43] D. K. Bowers, "Minimizing noise on analog bipolar circuit design," in *Proc. 1989 IEEE Bipolar Circuits Technol. Meet.*, 1989, pp. 107–111.
[44] P. R. Gray and R. G. Meyer, "Future directions in silicon IC's for RF personal communications," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1995, pp. 83–89.
[45] B. Razavi, "Challenges in portable RF transceiver design," *Circuits Devices*, vol. 12, no. 5, pp. 12–25, 1996.
[46] Z. Y. Chang and W. M. C. Sansen, *Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies*. Boston, MA: Kluwer , 1991, pp. 1–212.
[47] Z. Y. Chang, "Low-noise HF amplifiers," in *Analog Circuit Design " Low-Noise, Low-Power, Low-Voltage; Mixed-Mode Design with CAD Tools; Voltage, Current, and Time References*, J. H. Huijsing, R. J. van de Plassche, and W. M. C. Sansen, Eds. Boston, MA: Kluwer, 1996, pp. 3–26.
[48] H. J. Siweris and B. Schiek, "Analysis of noise upconversion in microwave FET oscillators," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 233–242, 1985.
[49] G. D. Vendelin, A. M. Pavio, and U. L. Rhode, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. New York: Wiley, 1990, pp. 418–442.
[50] O. Llopis, J. Verdier, R. Plana, and J. Graffeuil, "Low frequency noise in FET devices operated under nonlinear conditions consequences on oscillator phase noise," in *Conf. Proc. 25th Eur. Microwave Conf.*, 1995, pp. 285–289.
[51] M. N. Tutt, D. Pavlidis, A. Khatibzadeh, and B. Bayraktaroglu, "Investigation of HBT oscillator noise through $1/f$ noise and noise upconversion studies," *IEEE MTT-S Dig.*, vol. 2, pp. 727–730, 1992.
[52] ——, "The role of baseband noise and its upconversion in HBT oscillator phase noise," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 1461–1471, 1995.
[53] D. R. Pehlke *et al.*, "A predictive model describing the upconversion of $1/f$ noise into sideband noise in HBTs," in *Dig. 53rd Annu. Device Research Conf.*, 1995, pp. 94–95.
[54] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, pp. 329–330, 1966.
[55] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986, pp. 1–306.
[56] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331–343, 1996.
[57] ——, "Analysis, modeling, and simulation of phase noise in monolithic voltage-controlled oscillators," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1995, pp. 323–326.
[58] K. Bult *et al.*, "Low power system for wireless microsensors," in *Int. Symp. Low Power Electronics and Design (ISLEPD) Dig. Tech. Papers*, 1996, pp. 17–21.
[59] W. H. Press, B. P. Flannery, S. A. Teukolsky, and W. T. Vetterling, *Numerical Recipes in C: The Art of Scientific Computing*. Cambridge: Cambridge Univ. Press, 1990, pp. 523–528.
[60] J. Kilmer, A. Van der Ziel, and G. Bosman, "Presence of mobility fluctuation $1/f$ noise identified in silicon P^+NP transistors," *Solid-State Electron.*, vol. 26, pp. 71–74, 1983.
[61] H. A. W. Markus and T. G. M. Kleinpenning, "Low-frequency noise in polysilicon emitter bipolar transistors," *IEEE Trans. Electron Devices*, vol. 42, pp. 720–727, Apr. 1995.
[62] T. G. M. Kleinpenning, "Location of low-frequency noise sources in submicrometer bipolar transistors," *IEEE Trans. Electron Devices*, vol. 39, pp. 1501–1506, June 1992.
[63] A. van der Ziel, X. Zhang, and A. H. Pawlikiewicz, "Location of $1/f$ noise sources in BJT's and HBT's—I. Theory," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 1371–1375, Sept. 1986.
[64] A. H. Pawlikiewicz and A. van der Ziel, "Location of $1/f$ Noise Sources in BJT's and HBT's—II. Experiment," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 2009–2012, Sept. 1987.
[65] S. Tanaka, H. Shimawaki, K. Kasahara, and K. Honjo, "Characterization of current-induced degradation in be-doped HBT's based in GaAs and InP," *IEEE Trans. Electron Devices*, vol. 40, pp. 1194–1201, July 1993.
[66] L. S. R. Vempati, "Low-Frequency Noise in UHV/CVD Silicon and Silicon–Germanium Bipolar Transistors," Master's thesis, Auburn Univ., Auburn, AL, 1995.
[67] L. S. Vempati *et al.*, "Low-frequency noise in UHV/CVD epitaxial Si- and SiGe-base bipolar transistors," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1458–1467, 1996.
[68] A. K. Kirtania *et al.*, "Measurement and comparison of $1/f$ noise and g-r noise in silicon homojunction and III–V heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 43, pp. 784–792, May 1996.
[69] M. B. Das, "On the current dependence of low-frequency noise in bipolar transistors," *IEEE Trans. Electron Devices*, vol. ED-22, pp. 1092–1098, Dec. 1975.
[70] X. C. Zhu, A. Pawlikiewicz, and A. van der Ziel, "$1/f$ noise in n^+-p-n microwave transistors," *Solid-State Electron.*, vol. 28, pp. 473–477, 1985.

[71] E. Simoen *et al.*, "Impact of polysilicon emitter interfacial layer engineering on the $1/f$ noise of bipolar transistors," *IEEE Trans. Electron Devices*, vol. 43, pp. 2261–2268, Dec. 1996.

[72] S. Decoutere *et al.*, "Identification of $1/f$ diffusion and recombination noise sources in bipolar transistors," *IEDM Tech. Dig.*, pp. 25–28, 1990.

[73] J. W. M. Leach, "Fundamentals of low-noise analog circuit design," *Proc. IEEE*, vol. 82, pp. 1515–1538, 1994.

[74] A. H. Pawlikiewicz, A. van der Ziel, G. S. Kousik, and C. M. Van Vliet, "Fundamental $1/f$ noise in silicon bipolar transistors," *Solid-State Electronics*, vol. 31, no. 5, pp. 831–834, 1988.

[75] J.-H. Shin *et al.*, "Low-frequency noise characterization of self-aligned AlGaAs–GaAs heterojunction bipolar transistors with a noise corner frequency below 3 kHz," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1604–1613, 1998.

[76] M. J. Deen, S. Rumyantsev, R. Bashir, and R. Taylor, "Measurement and comparison of low frequency noise in npn and pnp polysilicon-emitter bipolar junction transistors," *J. Appl. Phys.*, vol. 84, pp. 625–633, 1998.

[77] J. D. Cressler *et al.*, "Low-frequency noise characteristics of UHV/CVD epitaxial Si- and SiGe-base bipolar transistors," *IEEE Electron Device Lett.*, vol. 17, pp. 13–15, Jan. 1996.

[78] X. Zhu and A. van der Ziel, "The hooge parameters of n^+-p-n and p^+-n-p silicon bipolar transistors," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 658–661, Mar. 1985.

[79] T. G. M. Kleinpenning, "On $1/f$ mobility fluctuations in bipolar transistors," *Physica B*, vol. 138, pp. 244–252, 1986.

[80] A. Mounib *et al.*, "Low frequency $(1/f)$ noise model for the base current in polysilicon emitter bipolar junction transistors," *J. Appl. Phys*, vol. 79, no. 6, pp. 3330–3336, 1996.

[81] A. Mounib, G. Ghibaudo, D. Pogany, and J. A. Chroboczek, "Aging and noise in the Si bipolar junction transistor," in *Sixth Quantum $1/f$ Noise and Other Low Frequency Fluctuations in Electronic Devices Symposium*, P. H. Handel and A. L. Chung, Eds. Woodbury, NY: AIP, 1996, vol. AIP Conf. Proc. 371, pp. 107–114.

[82] J.-M. Routoure *et al.*, "Crowding effects and low frequency noise in polysilicon emitter bipolar transistors," *Solid-State Electron.*, vol. 43, pp. 931–936, 1999.

[83] G. Blasquez, J. Caminade, and K. M. van Vliet, "An accurate analysis of noise in rectangular bipolar transistors including current crowding," *Solid-State Electron.*, vol. 23, pp. 423–431, 1980.

[84] H. A. W. Markus and B. J. J. Hanssen, "$1/f$ noise in bipolar transistors: Influence of emitter geometry, edge effects, and current crowding," in *Proc. 13th Int. Conf. Noise in Physical Systems and $1/f$ Fluctuations*, V. Bareikis and R. Katilius, Eds. Singapore: World Scientific, 1995, pp. 462–465.

[85] H. Higuchi and S. Ochi, "$1/f$ noise characteristics of bipolar transistors," in *Proc. Symp. $1/f$ Fluctuations*, Tokyo, Japan, 1977, p. 140.

[86] P. Llinares *et al.*, "Dimension scaling of $1/f$ noise in the base current of quasiself-aligned polysilicon emitter bipolar junction transistors," *J. Appl. Phys.*, vol. 82, no. 5, pp. 2671–2675, 1997.

[87] R. Gabl, K. Aufinger, J. Bock, and T. F. Meister, "Low-frequency noise characteristics of advanced Si and SiGe bipolar transistors," in *Proc. ESSDREC*, 1997, pp. 536–539.

[88] P.-F. Lu, "Low-frequency noise in self-aligned bipolar transistors," *J. Appl. Phys.*, vol. 62, pp. 1335–1339, 1987.

[89] M. J. Deen, J. Ilowski, and P. Yang, "Low frequency noise in polysilicon-emitter bipolar junction transistors," *J. Appl. Phys.*, vol. 77, pp. 6278–6288, 1995.

[90] G. D. Vendelin, A. M. Pavio, and U . L. Rhode, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. New York: Wiley, 1990, pp. 106–142.

[91] D. Harame, "High performance BiCMOS process integration: Trends, issues, and future directions," in *Proc. IEEE Bipolar Circuits Technol. Meet.*, 1997, pp. 36–43.

[92] T. G. M. Kleinpenning and A. J. Holden, "$1/f$ noise in n-p-n GaAs/AlGaAs heterojunction bipolar transistors: Impact of intrinsic transistors and parasitic series resistance," *IEEE Trans. Electron Devices*, vol. 40, pp. 1148–1153, June 1993.

[93] D. Costa, M. N. Tutt, A. Khatibzadeh, and D. Pavlidis, "Tradeoff between $1/f$ noise and microwave performance in AlGaAs/GaSa heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 41, pp. 1347–1350, Aug. 1994.

[94] P. O. Lauritzen, "Noise due to generation and recombination of carriers in p-n junction transition regions," *IEEE Trans. Electron Devices*, vol. ED-15, pp. 770–776, Oct. 1968.

[95] L. S. Vempati *et al.*, "Low-frequency noise in UHV/CVD Si- and SiGe-base bipolar transistors," in *Proc. 1995 IEEE Bipolar Circuits Technol. Meet.*, 1995, pp. 129–132.

[96] Y. Dai, "Deep-level impurity analysis for p-n junctions of a bipolar transistor from low-frequency g-r noise measurements," *Solid-State Electron.*, vol. 32, pp. 439–443, 1989.

[97] J. H. Shin *et al.*, "Low $1/f$ noise characteristics of AlGaAs/GaAs heterojunction bipolar transistor with electrically abrupt emitter-base junction," *IEEE Electron Device Lett.*, vol. 18, pp. 60–62, Feb. 1997.

[98] J. A. Babcock *et al.*, "$1/f$ noise in graded-channel MOSFET's for low-power low-cost RFICs," in *Device Research Conf. Dig.*, 1997, pp. 122–123.

[99] S. Tehrani *et al.*, "Low-frequency noise in heterojunction FET's with low-temperature buffer," *IEEE Trans. Electron Devices*, vol. 39, pp. 1070–1074, May 1992.

[100] X. C. Zhu, X. N. Zhang, A. van der Ziel, and C. O. Bozler, "Low-frequency noise in permeable base transistors," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 1408–1413, Oct. 1984.

[101] B. K. Jones and R. C. J. Smets, "The excess noise in silicon bipolar transistors," in *Noise in Physical Systems and $1/f$ Fluctuations*, P. H. Handel and A. L. Chung, Eds. Saint Louis, MO: AIP, 1993, vol. Conf. Proc. no. 285, pp. 240–243.

[102] A. J. Brodersen, E. R. Chenette, and R. C. Jaeger, "Noise in integrated-circuit transistors," *IEEE J. Solid-State Circuits*, vol. SC-5, pp. 63–66, 1970.

[103] R. C. Jaeger and A. J. Brodersen, "Low-frequency noise sources in bipolar junction transistors," *IEEE Trans. Electron Devices*, vol. ED-17, pp. 128–134, Feb. 1970.

[104] T. C. Verster, "Anomalies in transistor low-frequency noise," *Proc. IEEE*, vol. 55, pp. 1204–1205, July 1967.

[105] Y. Dai, "Optimal low-frequency noise criteria used as a reliability test for BJT's and experimental results," *Microelectron. Reliab.*, vol. 31, no. 1, pp. 75–78, 1991.

[106] Y. Dai and H. Chen, "Current noise due to generation and recombination of carriers in forward-biased p-n junctions," *Solid-State Electron.*, vol. 34, no. 3, pp. 259–264, 1991.

[107] G. Blasquez, "General aspects of noise phenomena—Application to surface noise," in *Instabilities in Silicon Devices, Silicon Passivation and Related Instabilities*, G. Barbottin and A. Vapaille, Eds. Amsterdam, The Netherlands: North-Holland, 1989, vol. 1, pp. 363–398.

[108] X. N. Zhang, A. van der Ziel, H. Duh K, and H. Morkoç, "Burst and low-frequency generation-recombination noise in double-heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 277–279, July 1984.

[109] D. C. Murray *et al.*, "Increase of low-frequency-noise-generating defects in today's CMOS and BiCMOS technologies," *Mat. Sci. Eng.*, vol. B4, pp. 367–372, 1989.

[110] X. L. Wu, A. van der Ziel, A. N. Bibbas, and A. D. van Rheenen, "Burst-type noise mechanisms in bipolar transistors," *Solid-State Electron.*, vol. 32, no. 11, pp. 1039–1042, 1989.

[111] J. C. Costa *et al.*, "Extracting $1/f$ noise coefficients for BJT's," *IEEE Trans. Electron Devices*, vol. 41, pp. 1992–1999, Nov. 1994.

[112] S. Machlup, "Noise in semiconductors: Spectrum of a two-parameter random signal," *J. Appl. Phys.*, vol. 25, no. 3, pp. 341–343, 1954.

[113] J. A. Copeland, "Semiconductor impurity analysis from low-frequency noise spectra," *IEEE Trans. Electron Devices*, vol. ED-18, pp. 50–53, Jan. 1971.

[114] H. Nii *et al.*, "A novel lateral bipolar transistor with 67 GHz $f_{\max}$ on thin film SOI for RF analog applications," *IEEE Trans. Electron Devices*, vol. 47, pp. 1536–1541, July 2000.

[115] F. Scholz, J. M. Hwang, and D. K. Schroder, "Low frequency noise and DLTS as semiconductor device characterization tools," *Solid-State Electron.*, vol. 31, pp. 205–217, 1988.

[116] J.-Q. Lú and F. Koch, "Random telegraph noise in advanced self-aligned bipolar transistors," *Jpn. J. Appl. Phys.* , pt. 1, vol. 35, pp. 826–832, 1996.

[117] B. Balland and G. Barbottin, *Trapping and Detrapping Kinetics Impact on C(V) and I(V) Curves, in Instabilities in Silicon Devices, Silicon Passivation and Related Instabilities*, G. Barbottin and A. Vapaille, Eds, Amsterdam, The Netherlands: North-Holland, 1989, vol. 2, pp. 19–69.

[118] R. Roedel and C. R. Viswanathan, "Reduction of popcorn noise in integrated circuits," *IEEE Trans. Electron Devices*, vol. ED-22, pp. 962–964, Oct. 1975.

[119] H. Khajezadeh and T. T. McCaffrey, "Material and process considerations for monolithic low-$1/f$ noise transistors," *Proc. IEEE*, vol. 57, pp. 1518–1522, 1969.

[120] M. Stoisiek and D. Wolf, "Effects of phosphorus gettering on $1/f$ noise in bipolar transistors," *Solid-State Electron.*, vol. 23, pp. 1147–1149, 1980.

[121] G. Ritter, K. E. Ehwald, and P. Schley, "Defect engineering for BiCMOS-technology," *Solid-State Phenomena*, vol. 6 & 7, pp. 57–63, 1989.
[122] N. Siabi-Shahrivar, W. Redman-White, P. Ashburn, and H. A. Kemhadjian, "Reduction of $1/f$ noise in polysilicon emitter bipolar transistors," *Solid-State Electron.*, vol. 38, pp. 389–400, 1995.
[123] P. Llinares *et al.*, "Low frequency $1/f$ noise characterization of advanced CMOS-compatible bipolar junction transistors for technology evaluation," in *Proc. ESSDREC*, 1997, pp. 532–535.
[124] R. Tang *et al.*, "Extrinsic base optimization for high-performance RF SiGe heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 18, pp. 426–428, Sept. 1997.
[125] R. Tang *et al.*, "Optimal extrinsic base fabrication for high performance SiGe HBT's for RF communication applications," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 1997, pp. 435–438.
[126] M. J. Deen, J. Ilowski, and P. Yang, "The effects of emitter geometry and device processing on the low frequency noise of polysilicon emitter npn bipolar transistors," in *Proc. 13th Int. Conf. Noise Physical Syst. $1/f$ Fluctuations*, V. Bareikis and R. Katilius, Eds. Singapore: World Scientific, 1995, pp. 454–457.
[127] N. Siabi-Shahrivar *et al.*, "The effects of scaling and rapid thermal annealing on the $1/f$ noise of polysilicon emitter bipolar transistors," *Microelectron. Eng.*, vol. 15, pp. 533–536, 1991.

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