The Role of the Mercury-Si Schottky-Barrier Height in Ψ-MOSFETs

J. Y. Choi, S. Ahmed, T. Dimitrova, J. T. C. Chen, *Member, IEEE*, and D. K. Schroder, *Life Fellow, IEEE*

***Abstract*—Pseudo-MOSFETs (Ψ-MOSFET) are routinely used for silicon-on-insulator (SOI) material characterization, allowing threshold voltage, electron and hole mobility, doping density, oxide charge, interface trap density, etc. to be determined. The HgFET, one version of the Ψ-MOSFET, uses mercury source and drain contacts. It is a very effective SOI test structure, but its current-voltage behavior is critically dependent on the Hg–Si interface. We have investigated this interface through current–voltage measurements of HgFETs and Schottky diodes and through device modeling. We show that modest barrier height changes of 0.2 eV lead to current changes of up to three orders of magnitude. Etching the Si surface in a mild HF : H_2O solution can easily change barrier heights and we attribute this behavior to Si surface passivation of dangling bonds. As this surface passivation diminishes with time, the Si surface becomes a more active generation site and the barrier height of the Hg–Si interface changes, taking on the order of 50–100 h at room temperature in air.**

***Index Terms*—Pseudo-MOSFET (Ψ-MOSFET), Schottky barrier, semiconductor device measurements, silicon, silicon-on-insulator (SOI) technology.**

I. INTRODUCTION

POINT-CONTACT and mercury-probe pseudo-MOSFETs (Ψ-MOSFET) have become routine silicon-on-insulator (SOI) characterization structures [1], [2]. They have the advantage of not requiring device fabrication; it is not even necessary to grow an oxide. Historically, the point contact Ψ-MOSFET was first used [3]. The mercury-probe configuration, called the HgFET, is a more recent innovation with the advantage of well-defined source and drain areas. It is well described by Hovel [4]. Being a Schottky contact source/drain device, its current–voltage (*I–V*) behavior is sensitive to the Hg–Si interface and its Schottky-barrier height. The Si surface is very important for the HgFET, since the Schottky-barrier is critically influenced by the Hg–Si interface. In this paper we discuss the Hg–Si barrier and its effect on the HgFET behavior. We do this through *I–V* measurements of Schottky-barrier diodes and HgFETs as well as through device modeling.

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II. Hg–Si INTERFACE

Mercury–silicon junctions are commonly used for epitaxial layer doping concentration measurements and SOI material characterization. The Hg–Si junctions form either Schottky or ohmic contacts, require neither elaborate sample preparation nor heat treatment and there is very little interaction of mercury with silicon. Our Rutherford backscattering spectroscopy measurements have not detected any mercury on the Si surface, even after touching the Hg probe six times on a given Si surface location. However, the Schottky-barrier behavior is extremely sensitive to the Hg–Si interface. Donald first reported measurements of Hg–Si contacts using n-Si and p-Si and formed Hg–Si contact by various means [5]. The barrier height of the Hg–Si junctions was found to be sensitive to the environment, i.e., the barrier height changed immediately when the samples were removed from the Hg into air. He did not report why that occurs. Severin and Poodt showed that n-Si wafers needed to be cleaned and boiled in HNO_3 or $H_2O_2 + H_2SO_4$ to grow a thin oxide layer for Hg–Si junctions to be rectifying [6]. If the wafers are etched in hydrogen fluoride (HF), ohmic contacts with low barrier height formed. For p-type wafers, they found Schottky-like behavior with or without the thin oxide. Wang *et al.* found they required a thin oxide (<2 nm) on n-Si for good Schottky diodes [7]. They suggest a thin oxide for both n-Si and p-Si. Hovel believes that the HF rinse removes the native oxide, and passivates the Si surface, leaving a low density of ionic surface charge [4]. These various experiments clearly indicate that the Si surface condition is very important for Hg–Si contacts.

The work function of mercury is 4.5 eV and the electron affinity of silicon is 4.05 eV. When Hg is brought into intimate contact with Si, with no interface states, according to the Schottky theory [8], the barrier height on n-Si, ϕ_{Bn}, is given by

$$\phi_{\mathrm{Bn}} = \phi_M - \chi = 0.45 \text{ eV} \tag{1}$$

where ϕ_{M} is the metal work function and χ, the semiconductor electron affinity. The p-Si barrier height therefore is

$$\phi_{Bp} = E_G - \phi_{Bn} = 0.67 \text{ eV} \tag{2}$$

for a room-temperature Si band gap of 1.12 eV.

The value of $\phi_{\mathrm{Bn}} = 0.45$ eV on n-Si is in agreement with measurement, where $\phi_{\mathrm{Bn}} = 0.47$ eV is the barrier height after etching the Si sample in NH_4F with the Si surface hydrogen terminated containing very few dangling bonds or surface states [9]. After etching and leaving the sample in air, the Si surface slowly oxidizes and the n-Si barrier height increases to

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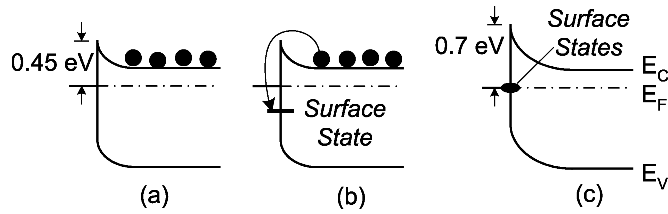

Fig. 1. Band diagram for (a) no interface states, (b) a surface state capturing an electron, and (c) a high density of surface states at $E_c - 0.7$ eV.

0.7 eV, presumably because the hydrogen-terminated Si surface is no longer passivated, and surface states form, leading to Fermi-level pinning. $\phi_{\rm Bp}$ should decrease to 0.42 eV when $\phi_{\rm Bn}$ increases to 0.7 eV.

A similar barrier height change has been reported for Al–n-Si Schottky barriers, where the barrier height changed from 0.45 to 0.7 eV after Al evaporation and aging at room temperature for about 100 h [10]. The proposed mechanism is a positive oxide charge in the thin oxide film (∼2 nm) between the Al and the Si that exists at the time of Al evaporation. This positive charge provides a dipole contribution, reducing the ideal barrier height. Thicker oxides lead to lower barrier heights. With aging, this positive charge dissipates and the true barrier height of 0.7 eV obtains. The charge dissipation mechanism was speculated to be due to electron injection from the Si substrate. For our Hg–n-Si case, we assume there is no oxide immediately after HF etch and as the oxide forms, the barrier height reduces. Hence, we believe the mechanisms in these two cases to be different.

Why does $\phi_{\rm Bn}$ change? We propose a possible explanation. Fig. 1(a) shows the band diagram immediately after HF or NH_4F etch with its 0.45 eV barrier height. We believe the Si surface to be hydrogen terminated with most of its surface states passivated by hydrogen. After exposing the H-terminated sample to air, the barrier height changes and the Hg–Si contact angle increases from 121° to 151° [9]. Clearly, the Hg–Si interface changes physically and electrically. During room-temperature oxidation, Si–Si and Si–H bonds at the surface are converted to Si–O bonds. However, similar to thermal oxidation at elevated temperatures, some Si bonds remain "unbonded," becoming interface states. We believe these to be surface generation sites or surface states. These surface states are likely to be the cause of Schottky-barrier height changes. Let us consider the formation of surface states in Fig. 1(b). If these states are acceptor-like, they capture electrons from the Si substrate, leading to increased barrier height. With time, the surface state density increases and finally saturates leading to Fermi-level pinning [11], from the initial 0.45-eV barrier height to 0.7 eV, indicated in Fig. 1(c).

Are surface states generated during room temperature oxidation? In an earlier paper, we showed that the effective SOI film generation lifetime ($\tau_{\rm geff}$), determined with the pulsed point-contact Ψ-MOSFET, varies with time following HF passivation [12]. In this technique, the substrate potential is pulsed, driving the Si film into deep depletion. The resulting electron-hole pair generation leads to a time-dependent drain current, from which the effective generation lifetime is determined [13]. The electron-hole pair generation takes place within the Si film, at the Si/buried oxide interface, and at the Si surface. After HF passivation, surface generation is low because there are few surface states. As the passivation loses its effectiveness, surface generation becomes active and $\tau_{\rm geff}$ decreases from 4 μs and saturates at 0.17 μs after about 100 h. The $\tau_{\rm geff}$ behavior is repeatable when the wafer is again rinsed in dilute HF. We found analogous behavior for SIMOX and bonded wafers and for dilute HF and dilute iodine surface rinses. We believe the effective generation lifetime behavior is caused primarily by the Si surface between source and drain point contacts, not by the contacts themselves. This surface changes with time, generating surface states, which, in turn, increase the surface electron-hole pair generation rate. It is very likely that similar surface changes affect the Hg–Si interface.

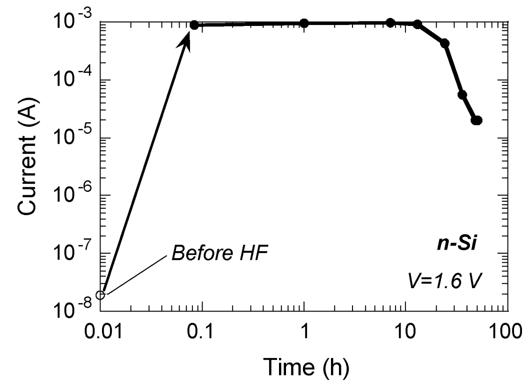

Fig. 2. Forward Schottky diode current as a function of time after dilute HF etch.

Fig. 2 shows the forward-bias current of an Hg–Si Schottky diode on an n-Si substrate. The current is initially very low, jumps to 0.9 mA after dilute HF etch and then gradually declines. This behavior is similar to the pulsed Ψ-MOSFETs measurements for an entirely different structure. Instead of surface generation rate affected by the HF etch, in Fig. 2 it is the barrier height that is changed. For the measurements in Fig. 2, Hg contact was made for the measurements. The probe was lifted between measurements. Hence, the Si surface was exposed to air most of the time, except for the measurement times when the Hg probe contacted the surface.

III. HgFET

The HgFET is a version of the Schottky MOSFET in Fig. 3, consisting of a *bulk* p-type substrate with Schottky source and drain contacts, first proposed by Lepselter and Sze and later modified and demonstrated by others [14]–[19]. The band diagrams near the surface are shown in Figs. 3 for zero, negative, and positive gate voltages. For drain current to flow with negative gate voltage, the *hole* barrier height $\phi_{\rm Bp}$ should be low, whereas for *positive* gate voltage the *electron* barrier height $\phi_{\rm Bn}$ should be low, illustrating the conflicting barrier height requirements for positive and negative gate voltages.

According to the earlier discussion of the barrier dependence on HF passivation, we have the situation in Fig. 4 for $+V_G$. For high $\phi_{\rm Bn}$, the drain current is low, because it is difficult to inject electrons from the source over the high barrier. For low $\phi_{\rm Bn}$, the drain current should be high, because now the barrier for electron injection is significantly lowered. This, indeed, is what we

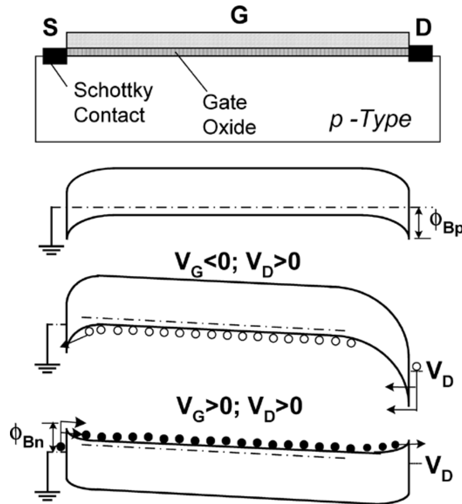

Fig. 3. Schottky MOSFET cross section, and band diagrams for $V_G > 0$ and $V_G < 0$.

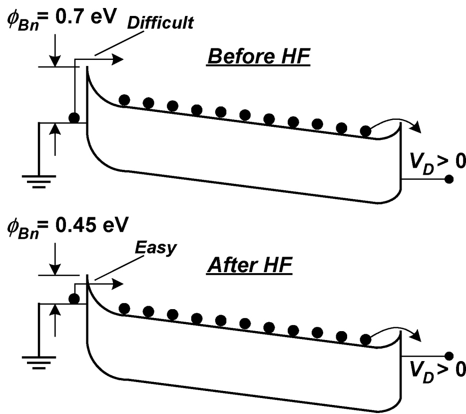

Fig. 4. Schottky MOSFET band diagrams for $+V_G$ and for high and low $\phi_{\rm Bn}$. These diagrams are believed to correspond approximately to "before" and "after" dilute HF etch.

observe, as shown in Fig. 5, where before HF etch the drain current is low for $+V_G$ and after HF etch it is high. "After HF etch" means the sample was measured about 5 min after the HF etch. Fig. 5 clearly illustrates the effect of barrier height, where before HF etch, $\phi_{\rm Bn}$ is high, leading to low *electron* drain current (+V) and $\phi_{\rm Bp}$ is low, leading to high *hole* current $(-V_G)$. After HF etch these barrier heights reverse.

The HgFET structure, illustrated in Fig. 6, consists of an SOI wafer with the substrate being the gate, the buried oxide being the gate oxide and the Si film being the body. It is similar to the devices discussed by Hovel [4]. Source and drain are formed by Hg pressure contacts in the Four Dimensions CV Map 92-B system. The system features a recycling Hg flow through the probe contacts to provide continuous cleaning of the metal fluid. The mercury probe is made up of a central circular dot serving as the source and a horseshoe-shaped ring as the drain. The Hg probe contacts the sample facing down, while the wafer back is contacted by a metal chuck and is biased as the gate. The SOI wafers in our experiments consisted of SIMOX and bonded wafers with Si film thicknesses ranging from 19 to 220 nm and buried oxide (BOX) thicknesses from 110 to 400 nm. In this paper, we report only on those measurements that illustrate the effects of the Hg–Si contacts. Effects due to BOX and edge leakage currents are not considered here.

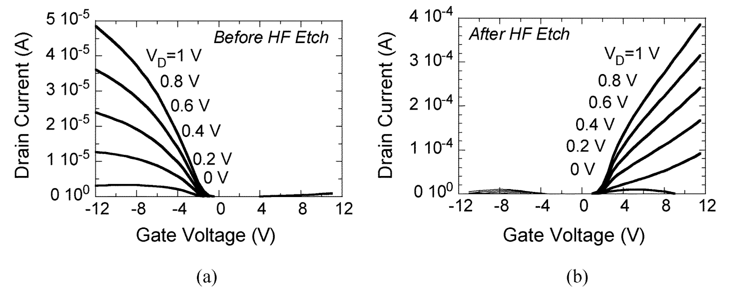

Fig. 5. Measured drain current-gate voltage characteristics for $+V_D$ for an HgFET (a) before and (b) after dilute HF etch. $t_{\rm Si} = 160$ nm, $t_{\rm BOX} = 145$ nm, $\rm N_{film} = 10^{15}$ cm^{-3}, and $\rm N_{sub} = 10^{15}$ cm^{-3}.

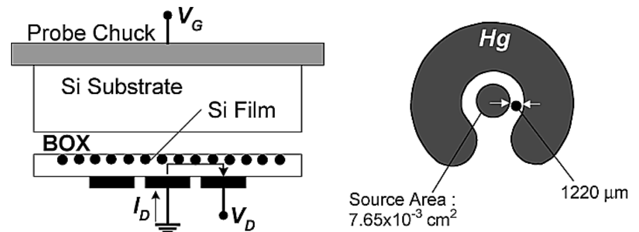

Fig. 6. HgFET and the Hg probe geometry.

We measure the drain current-gate voltage characteristics before any surface treatment. This is the "before HF etch" in the figures. The SOI wafer, without back surface metallization, is placed directly on the chuck of the probe system. Since the Si substrate is the gate of the HgFET with very low or zero gate current, we have not found it necessary to metallize the Si substrate. Then, we etch the SOI wafer in 1:20 HF : H_2O solution for 1 min and continue the measurements. It takes us about 5 min from the time of HF etching to the first measurement. In some cases we measure directly on an entire wafer, in some cases we etch the Si film into islands to eliminate leakage currents around the edge of the wafer and reduce leakage current through the buried oxide.

In addition to measurements, we have also simulated the HgFET. A detailed pseudo-MOSFET simulation was presented earlier by Munteanu *et al.*, concentrating on the *I–V*, mobility, geometrical effects, etc. [20] Although their simulations had electrodes with adjustable metal–semiconductor work functions, nothing was said of the effect of varying the work functions. Our simulations and measurements, on the other hand, are mainly concentrated on the effects of work function changes. In that sense, these two studies complement one another.

The structure considered for our SILVACO Atlas simulations consists of the Si film, the buried oxide and the substrate. Care was taken for fast and accurate simulations with a dense discretization mesh by scaling down the size of the source/drain contact regions and taking an equivalent two-dimensional structure of the circularly shaped device. Conventional models were used for the carrier statistics, generation-recombination, and mobility. Since we were mainly interested in the drain current dependence on barrier height, we simulated this effect. In Fig. 7, we show the effect of barrier height on both electron

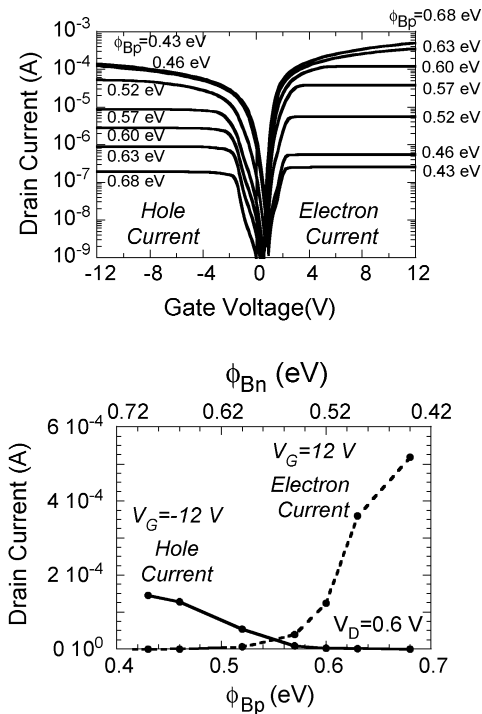

Fig. 7. Simulated I_D–V_G characteristics for a HgFET showing the effect of barrier height on electron and hole currents. $t_{\rm film} = 160$ nm, $N_{\rm film} = 10^{15}$ cm^{-3}, $N_{\rm sub} = 10^{15}$ cm^{-3}, and $V_D = 0.6$ V.

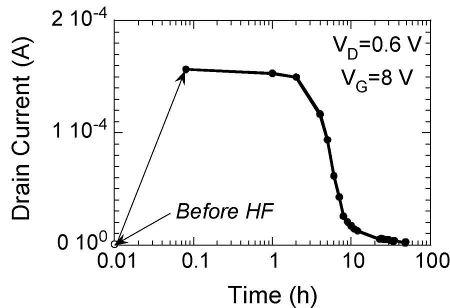

Fig. 8. Measured drain current versus time for a HgFET before and after dilute HF etch. 200-mm-diameter bonded p-Si, $t_{\rm film} = 160$ nm, $t_{\rm BOX} = 145$ nm, and $N_{\rm film} = 10^{15}$ cm^{-3}.

and hole currents. Note the strong influence of barrier height, with ϕ_B changes of 0.2 eV leading to drain current changes of 1000 $\times$. When one current type increases, the other decreases, as one would expect from Fig. 4. The barrier heights during the experimental measurements are, of course, unknown. However, the measured drain current versus time is shown in Fig. 8 after HF etch. These electron drain currents ($V_G = 8$ V) illustrate the effect of barrier height. Initially, $\phi_{\rm Bn}$ is low ($\phi_{\rm Bp}$ is high) leading to high drain current. With time, as the barrier height changes, I_D decreases as also shown in Fig. 7.

IV. Conclusion

The HgFET characterization of SOI wafers is very sensitive to the surface condition of the Si surface. For p-Si we find high drain current before dilute HF etch (1:20 HF : H_2O) for negative gate voltages and low drain current for positive gate voltages. The opposite behavior is observed after HF etch. We find similar behavior for Hg–Si Schottky-barrier diodes and attribute it to the passivation and depassivation of surface states. The HF etch passivates Si surface states. With time, an oxide grows on the HF-passivated surface. We believe this combination oxide growth and surface state passivation/depassivation changes the barrier height of the Hg–Si Schottky barrier, thereby influencing the drain current. Numerical simulations have confirmed and clarified the experimental trends. While oxide charges in the thin native oxide cannot be ruled out, we believe that surface states play the dominant role. This is particularly evident from the pulsed drain current effective generation lifetime data that are sensitive to surface generation sites. These measurements lead to an interface state density of around 10^{12}cm^{-2}eV^{-1}, sufficiently high to lead to Fermi level pinning of Schottky contacts, as suggested in Fig. 1. Overall we find behavior similar to Hovel's [4]: "An ionic charge, probably H^+ ions, is also adsorbed onto the Si surface, and is present on both the "free" Si surface and between the Hg and Si during the measurement. The HF ion-Hg combination acts as a low barrier height and low resistance Schottky barrier, in effect a quasi-ohmic contact. As time goes on, the charge dissipates and the device properties change accordingly, reaching a steady state after a number of hours."

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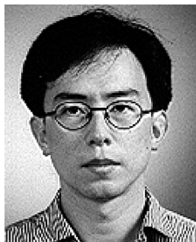

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