Low-Frequency Noise in Near-Fully-Depleted TFSOI MOSFET's

Jeffrey A. Babcock, Dieter K. Schroder, and Ying-Che Tseng

Abstract— **Low-frequency $(1/f)$ noise in near-fully-depleted Thin-Film Silicon-On-Insulator (TFSOI) CMOS transistors designed for sub-1-V applications is investigated in the subthreshold region, linear region, and saturation region of operation for the first time. The noise in these surface-channel devices is composed of a bias invariant $1/f$ component and a bias dependent generation-recombination (G/R) component that becomes enhanced in the subthreshold region of operation for both n- and p-channel MOSFET's. Results presented in this letter are consistent with the noise being dominated by a number fluctuation model. These results demonstrate that the bias independent $1/f$ noise spectrum of the n-channel TFSOI MOSFET is comparable to the $1/f$ noise level found in conventional bulk silicon submicron CMOS fabrication processes.**

I. Introduction

TECHNOLOGIES capable of delivering suitable RF-mixed mode IC operation at supply voltages of 1.0 V will become increasingly critical for the rapidly growing portable communications market [1], [2]. Recently, Thin-Film Silicon-On-Insulator (TFSOI) has emerged as a key technology capable of operating at supply voltages of 1.0 V, while maintaining performance advantages for low-power, low-cost, mixed-mode RFIC portable communications applications. This has been recently demonstrated by a sub-1-V microcontroller CPU which achieved a 2× improvement in clock frequency when compared to bulk silicon performance, while also attaining the high yield and low production costs required for large scale manufacturability [3], [4]. One of the critical measures of the electrical performance of a device is the low-frequency (LF) noise produced during circuit operation because it places a fundamental limit on signal detection and spectral purity. For low-voltage analog circuit operation, which dictates tighter control on circuit performance, LF noise becomes even more important. This is especially critical in low-power RF applications such as mixers and VCO's where $1/f$ noise becomes up-converted to the higher frequencies as phase noise [5]. Although much work has been done on TFSOI [6]–[8], very little exists on the noise properties of these devices [9]–[13]. In this letter, we give the first results on the noise properties of n- and p-channel MOSFET's designed for sub-1-V RF mixed-mode circuit applications [3], [14].

Manuscript received May 28, 1997.

J. A. Babcock and D. K. Schroder are with the Center for Solid-State Electronics Research, Department of Electrical Engineering, Arizona State University, Tempe, AZ 85287-5706 USA.

Y.-C. Tseng is with the Department of Electrical Engineering, University of California, Los Angeles, CA 90095 USA.

Publisher Item Identifier S 0741-3106(98)01359-7.

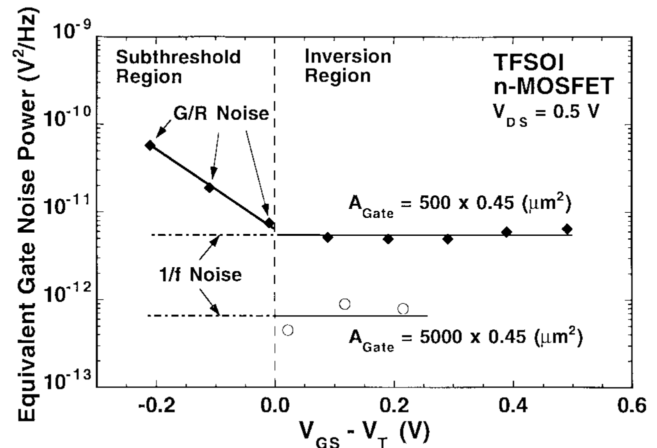

Fig. 1. Magnitude of the measured input-referred gate voltage noise power spectrum at 1.0 Hz for a small area ($A_{\mathrm{Gate}} = 10 \times 50 \times 0.45\ \mu\mathrm{m}^2$) and larger area ($A_{\mathrm{Gate}} = 100 \times 50 \times 0.45\ \mu\mathrm{m}^2$) n-channel MOSFET as a function of $V_{\mathrm{GS}} - V_T$. Note the increase in noise in the subthreshold region of operation is due to the appearance of G/R noise superimposed on the fundamental $1/f$ noise of the device.

II. Device Technology

Fabrication of the CMOS technology on TFSOI have been described by Huang *et al.* [15]. The technology is based on a fully manufacturable process with 0.5-μm CMOS devices [16] built on SIMOX substrates with a nominal Si thickness of 1000 Å and buried oxide thickness of 4000 Å. Titanium silicide source drain contacts are used to enhance high-frequency performance. Gate oxide thickness is 105 Å. Polysilicon-buffered LOCOS field isolation is used to isolate MOS devices [4].

LF noise measurements were made using a HP 3561A Dynamic Signal Analyzer with the gate electrode of the MOSFET ac shorted to ground. A wire wound load resistor was adjusted to achieve the desired drain-to-source voltage (V_{DS}). Noise signal amplification was provided by a EG&G Low Noise Amplifier model 113. An in-house specialized computer program controlled the equipment interface and calculated the input equivalent gate voltage noise source (S_{VG}) based on the device transconductance ($G_m = \Delta I_{\mathrm{DS}}/\Delta V_{\mathrm{GS}}$), the device output conductance ($G_{\mathrm{DS}} = \Delta I_{\mathrm{DS}}/\Delta V_{\mathrm{DS}}$), and the load resistance values [17].

III. Results

CMOS TFSOI device characteristics have been described in [16]. Noise characteristics of these transistors were measured

0741–3106/98$10.00 © 1998 IEEE

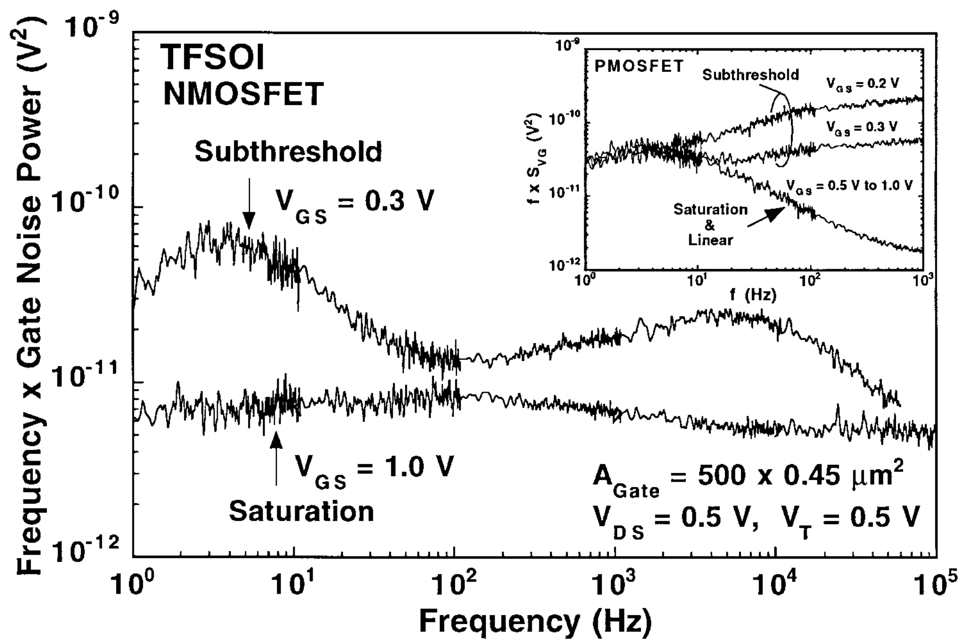

Fig. 2. Equivalent input-referred gate noise power spectral density multiplied by frequency ($S_{VG} \times f$) versus measured frequency for a TFSOI n-channel MOSFET biased in both the subthreshold and saturation regions of operation. Inset shows gate $S_{VG} \times f$ versus measured frequency for a TFSOI p-channel MOSFET also biased in both the subthreshold and saturation regions of operation.

at a constant $V_{\rm DS}$ of 0.5 and 1.0 V while the devices were operated in both the subthreshold and saturation regions of operation as a function of the gate voltage ($V_{\rm GS}$) and threshold voltage (V_T) difference. The drain currents ranged from 1.0 μA to 16 mA for the n-MOS and from 4.0 μA to 7.0 mA for the p-MOS, for these noise measurements. Noise in the linear region of operation was obtained by reducing $V_{\rm DS}$ to values less than $V_{\rm GS} - V_T$.

S_{VG} measured at 1.0 Hz for the n-MOS transistor with different gate area is shown in Fig. 1 as a function of $V_{\rm GS} - V_T$ at a constant $V_{\rm DS} = 0.5$ V. From these data, the input-referred $1/f$ noise in the n-MOSFET is independent of gate bias condition when the channel is inverted [9]. We also see the expected $1/Area$ dependence in the $1/f$ noise. In the subthreshold region of operation, $V_{\rm GS} - V_T < 0$, the noise at 1.0 Hz increases monotonically as $V_{\rm GS}$ is further decreased. The increase in LF noise during subthreshold operation is the result of G/R noise.

This effect of G/R noise can be easily seen in Fig. 2 where the input-referred noise multiplied by the frequency ($S_{VG} \times f$) is plotted versus frequency for a n-MOSFET [18], [19]. In saturation, $S_{VG} \times f$ is virtually independent of frequency. It can be inferred that the noise in this region is composed primarily of "pure" $1/f$ noise with only minor G/R noise present. However, when the device is operated in the subthreshold regime, we see the appearance of two distinct G/R noise centers, observed by the two Lorentzian shaped humps in the subthreshold noise, with $f_{GR1} \approx 3.5$ Hz and $f_{GR2} \approx 6.0$ kHz. It is clear that the G/R noise yields approximately an order of magnitude increase in the total noise measured at 1.0 Hz, when compared to the "pure" $1/f$ noise produced in the saturation region of operation. If we extrapolate the fundamental $1/f$ noise in the subthreshold region to its 1.0 Hz value, we see that the bias dependence of this noise source is almost identical to the $1/f$ noise measured in the saturation region of operation. This is represented by the dashed line showing $1/f$ noise in Fig 1.

Similar bias dependence and noise characteristics were observed in the TFSOI surface-channel p-MOSFET's as can be seen in the inset of Fig. 2. Fig. 3 compares the low-frequency noise measured in a p-MOS device to that in a n-MOS devices both operated at $V_{\rm GS} = 1.0$ and $V_{\rm DS} = 0.75$ V. The increased noise level at 1.0 Hz for the p-MOSFET's when compared to n-MOSFET's is attributed to the exponent $\lambda > 1.0$ in the $1/f^{\lambda}$ spectrum while the n-MOSFET's showed $\lambda < 1.0$ in the $1/f^{\lambda}$ spectrum. These results are similar to results we have obtained on bulk silicon surface-channel p-MOSFET's [20]. As in the case of the n-channel device, the p-MOSFET's showed enhanced noise when operated in the subthreshold regime. For the p-MOS devices the additional noise in the subthreshold region appeared as a shift in the noise power spectral density to $\lambda < 1.0$ in the $1/f^{\lambda}$ spectrum at higher frequencies. However, below approximately 10.0 Hz, the noise was found to be invariant with the applied voltage when the p-MOSFET's were operated in the saturation, linear, and subthreshold regions.

The fundamental $1/f$ noise (before the onset of the kink region, $V_{\rm DS} \leq 1.2$ V) remained bias independent both in the saturation and linear regions of operation with only a slight increase in G/R noise observed in the linear region of operation [13]. These results are consistent with those reported in bulk silicon where the equivalent input noise shows only minor variation with gate bias condition [17], [21]. Because the equivalent input noise contains a fundamental $1/f$ noise component that is independent of the applied voltage ($V_{\rm GS} - V_T$), we conclude that the LF noise sources in these

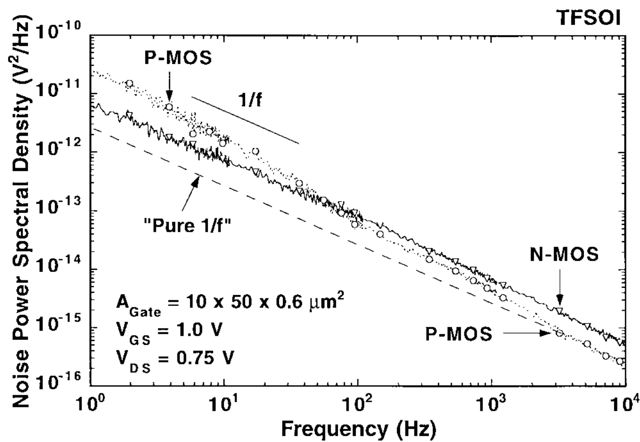

Fig. 3. Equivalent input-referred gate noise power spectral density versus measured frequency for a typical surface channel TFSOI n- and p-MOSFET ($A_{\rm Gate} = 10 \times 50 \times 0.45\ \mu{\rm m}^2$) both biased in the saturation regions with $V_{\rm GS} = 1.0$ V and $V_{\rm DS} = 0.75$ V.

devices is governed by the McWhorter number fluctuation model [22]–[24], and therefore can be predicted by a standard gate noise model of the form

$$S_{VG} = \frac{K_F}{C_{\rm OX}^2 \cdot W \cdot L_{\rm EFF} \cdot f}$$

where K_F is a noise magnitude constant which depends on the quality of the gate oxide, $C_{\rm OX}$ is the gate oxide capacitance per unit area, W is the channel width, $L_{\rm EFF}$ is the effective channel length, and f is the frequency. From the measured data in Fig. 1, we find $K_F \approx 1.2 \times 10^{-8}$ fC$^2/\mu$m for the n-channel TFSOI MOSFET's investigated in this work. This value is exceptionally close to the $1/f$ noise level found in a typical CMOS fabrication processes where $K_F \approx 5 \times 10^{-9}$ fC$^2/\mu$m on the average for n-channel MOSFET's [25].

IV. Conclusions

We have examined LF noise as a function of bias condition in the subthreshold region, linear region, and saturation region of operation in surface-channel TFSOI n- and p-MOSFET's for the first time. Results indicate that the LF noise in n-MOSFET's are composed of fundamental bias invariant $1/f$ noise and G/R noise which depends on the gate bias and becomes enhanced in the subthreshold region of operation. A similar bias dependence has been observed in the p-MOSFET's, except in the subthreshold region, the enhanced noise was due to a shift in the noise power spectral density to $\lambda < 1.0$ in the $1/f^\lambda$ spectrum at higher frequencies indicating a shift in the trapping processes involving short time constants [26]. The bias independence of the input-referred $1/f$ noise gives strong evidence for McWhorter's surface number fluctuations model governing the noise characteristics of these devices. Because G/R noise is enhanced in the subthreshold region of operation, care should be taken when designing low-noise analog applications that need to operate in this region. However, for most other applications which operate in the saturation region, the low-frequency noise is governed by fundamental $1/f$ noise which is bias invariant and thus can be predicted for sub-1-V RF mixed-mode applications. Finally, it has been demonstrated that the $1/f$ noise level found in these TFSOI near-fully-depleted n-channel MOSFET's is comparable to that found in typical bulk silicon CMOS fabrication processes.

Acknowledgment

The authors gratefully acknowledge the technical contributions of J. Ford, M. Huang, D. Ngo, S. Cheng, and D. Monk. They also thank Motorola CPL for providing the TFSOI samples.

References

[1] S. Urabe and T. Nojima, "Developments in mobile/portable telephones and key devices for miniaturization," in *IEICE Trans. Electron.*, vol. E79-C, no. 5, pp. 600–605, 1996.

[2] B. Davari, R. H. Dennard, and G. G. Shahidi, "CMOS scaling for high-performance and low-power—The next ten years," *Proc. IEEE*, vol. 83, pp. 595–606, 1995.

[3] W.-L. M. Huang, K. Papworth, M. Racanelli, J. P. John, J. Foerstner, H. C. Shin, H. Park, B. Y. Hwang, T. Wetteroth, S. Hong, H. Shin, S. Wilson, and S. Cheng, "TFSOI CMOS technology for sub-1-V microcontroller circuits," in *IEDM Tech. Dig.*, 1995, pp. 59–62.

[4] M. Racanelli, W.-L. M. Huang, H. C. Shin, J. Foerstner, B. Y. Hwang, S. Cheng, P. L. Fejes, H. Park, T. Wetteroth, S. Hong, H. Shin, and S. R. Wilson, "Controlling the device field edge to achieve a low-power TFSOI technology," in *IEDM Tech. Dig.*, 1995, pp. 885–888.

[5] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, pp. 329–330, 1966.

[6] J. P. Colinge, "Recent advances in SOI technology," in *IEDM Tech. Dig.*, 1994, pp. 817–820.

[7] P. K. Vasudev, "CMOS devices and interconnect technology enhancements for low-power/low-voltage applications," *Solid-State Electron.*, vol. 39, no. 4, pp. 481–487, 1996.

[8] M. Yoshimi, M. Terauchi, A. Murakoshi, M. Tekahashi, K. Matsuzawa, N. Shigyo, and Y. Ushiku, "Technology trends of silicon-on-insulator—Its advantages and problems to be solved," in *IEDM Tech. Dig.*, 1994, pp. 429–432.

[9] J. Hsu, J. Wang, J. Woo, and C. R. Viswanathan, "Flicker noise in thin-film fully-depleted SOI MOSFET's," in *Proc. IEEE Int. SOI Conf.*, 1991, pp. 30–31.

[10] N. Lukyanchikova, M. Petrichuk, N. Garbar, E. Simoen, and C. Claeys, "Back and front interface related generation-recombination noise in buried channel SOI pMOSFET's," *IEEE Trans. Electron Devices*, vol. 43, pp. 417–423, Mar. 1996.

[11] E. Simoen and C. Claeys, "The low-frequency noise behavior of silicon-on-insulator technologies," *Solid-State Electron.*, vol. 39, no. 7, pp. 949–960, 1996.

[12] T. Elewa, B. Boukriss, H. S. Haddara, A. Chovet, and S. Cristoloveanu, "Low-frequency noise in depletion-mode SIMOX MOS transistors," *IEEE Trans. Electron Devices*, vol. 38, pp. 323–327, 1991.

[13] J. A. Babcock, W. M. Huang, J. M. Ford, D. Ngo, D. J. Spooner, and S. Cheng, "Low-frequency noise dependence of TFSOI BiCMOS for low-power RF mixed mode applications," in *IEDM Tech. Dig.*, 1996, pp. 133–136.

[14] W. M. Huang, D. Ngo, J. Babcock, H.C. Shin, P. Welch, M. Racanelli, J. Foerstner, J. Ford, and S. Cheng, "TFSOI complementary BiCMOS technology for low-power RF mixed-mode applications," in *IEEE CIC Conf.*, 1996, pp. 35–38.

[15] W.-L. M. Huang, K. M. Klein, M. Grimaldi, M. Racanelli, S. Ramaswami, J. Tsao, J. Foerstner, and B.-Y. C. Hwang, "TFSOI complementary BiCMOS technology for low-power applications," *IEEE Trans. Electron Devices*, vol. 42, pp. 506–512, Mar. 1995.

[16] B.-Y. Hwang, M. Racanelli, M. Huang, J. Foerstner, S. Wilson, T. Wetteroth, S. Wald, J. Rugg, and S. Cheng, "SOI for low-power applications," in *Ext. Abstr. Int. Conf. Solid-State Devices Mater.*, 1994, pp. 268-270.

[17] N. Mutoh and N. Teranishi, "New empirical relation for MOSFET $1/f$ noise unified over linear and saturation regions," *Solid-State Electron.*, vol. 31, no. 12, pp. 1675–1680, 1988.

[18] B. Hughes, N. G. Fernandez, and J. M. Gladstone, "GaAs FET's with a flicker-noise corner below 1 MHz," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 733–741, 1987.

[19] Y. Dai, "A precision noise measurement and analysis method used to estimate reliability of semiconductor devices," *Microelectron. Reliab.*, vol. 37, no. 6, pp. 893–899, 1997.

[20] J. A. Babcock, C. E. Gill, J. M. Ford, D. Ngo, E. Spears, J. Ma, H.-B. Liang, D. J. Spooner, and S. Cheng, "$1/f$ noise in graded-channel MOSFET's for low-power low-cost RFIC's," in *Tech. Dig. Device Res. Conf.*, 1997, pp. 123–124 (additional results unpublished).

[21] M. Aoki, Y. Sakai, and T. Masuhara, "Low $1/f$ noise design of hi-CMOS devices," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 296–299, 1982.

[22] A. van der Ziel, "Flicker noise in electronic devices," *Adv. Electron. Electron Phys.*, vol. 49, pp. 225–297, 1979.

[23] S. Christensson, I. Lundström, and C. Svensson, "Low-frequency noise in MOS transistors—Part I: Theory," *Solid-State Electron.*, vol. 11, pp. 797–812, 1968.

[24] A. L. McWhorter, "$1/f$ noise and germanium surface properties," in *Semiconductor Surface Physics*, R. H. Kingston, Ed. Philadelphia, PA: Univ. Pennsylvania Press, 1957, pp. 207–228.

[25] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.

[26] C. Surya and T. Y. Hsiang, "Theory and experiments on the $1/f^{\gamma}$ noise in p-channel metal-oxide-semiconductor field-effect transistors at low drain bias," *Phys. Rev. B*, vol. 33, no. 7, pp. 4898–4905, 1986.