Post Poly-Si Gate Rapid Thermal Nitridation for Boron Penetration Reduction and Oxide Reliability Improvement

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***Abstract*— Boron penetration from p$^+$ doped poly-Si gates in PMOSFET is greatly reduced by post poly-Si gate rapid thermal nitridation. Gate oxide reliability against boron penetration is significantly enhanced. When post poly-Si nitridation is combined with N_2O annealed gate oxides, gate oxide charge-to-breakdown is markedly improved.**

I. Introduction

BORON penetration in PMOSFET's with p$^+$ doped poly-Si gates has been studied extensively. Boron penetration in PMOSFET's can cause threshold voltage instability, subthreshold slope (SS) and gate transconductance degradation, and additional interface state generation [1]–[3]. Gate oxide reliability was found to degrade due to boron penetration into the oxide [4]. Oxide nitridation has reduced boron penetration and improved gate oxide charge-to-breakdown ($Q_{\rm bd}$) [5]–[7]. Post poly-Si gate nitridation reduces boron penetration from p$^+$ poly-Si gates into the oxide. Consequently gate oxide reliability against boron penetration is improved. Gate oxide $Q_{\rm bd}$ improvement is greatest when post poly-Si gate nitridation is combined with nitrided gate oxide.

II. Experimental

MOS-C's and PMOSFET's were fabricated on (100) p-type Si substrate with a 14–22 Ω-cm resistivity. N-well is formed by a 4.0×10^{12} cm^{-2}, 10 keV phosphorous implant. Thermal oxide is grown at 830 °C to form the gate oxide. Some wafers are annealed in a N_2O ambient at the same temperature (830 °C) for 30 min following thermal oxidation. The gate oxide thickness for both thermal and N_2O annealed oxides is 97 Å determined by ellipsometry. Poly-Si gates are deposited in two steps: 550 Å first deposition, followed by 2750 Å second deposition. The two step poly-Si process provides process convenience of performing V_t adjust implant (1.5×10^{12} cm^{-2}, 60 keV Phosphorous in our experiment) after the first poly-Si deposition. Some wafers receive RTP nitridation after first 550 Å poly-Si deposition in pure NH_3 for 3 min at temperatures of 1050 and 850 °C. A 100 : 1 HF clean follows the poly-Si nitridation step. PMOSFET's are formed by 5.0×10^{15} cm^{-2}, 65 keV BF_2 source/drain implant, which simultaneously dopes the poly-Si gates. All wafers receive a 10-min poly-Si oxidation process at 900 °C after the gate patterning, therefore all wafers are subject to some degree of boron penetration. An additional 850 °C, 15 min drive-in process is performed on some wafers to accelerate boron penetration.

Capacitors have an area of 3.2×10^{-4} cm^{-2}. MOSFET's have drawn gate lengths of 0.8 μm. MOS-Cs were F–N stressed in accumulation mode at a constant current density of 100mA/cm^2.

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III. Results and Discussions

Table I shows the experiment matrix and corresponding PMOSFET's parameter shift due to 850 °C boron drive-in process. Data was taken from five sites per wafer for each experimental condition. Numbers in Table I are averages of the data points for each split. Parameter shift is noted as negligible when there is no significant statistical difference between the data population [8]. Both N_2O annealed oxides and nitridation of poly-Si gates reduce boron penetration. When poly-Si gate nitridation is combined with N_2O annealed oxides, boron penetration is not observed based on PMOSFET's I–V characteristics (V_t, g_m, and SS). These data shows that N_2O annealed oxides are able to prevent boron diffusing into the substrate, for the drive-in temperature range studied, due to the nitrogen rich layer at the SiO_2/Si interface [9]. Post poly-Si gate NH_3 nitridation further reduces boron penetration into the gate oxide when combined with N_2O annealed oxides. Fig. 1 shows the high and low frequency C–V curves comparing poly-Si gate with and without NH_3 nitridation. The C–V curves closely resembles each other. The insert in Fig. 1. shows the comparison of sheet resistance of p type poly-Si with and without NH_3 nitridation, and no statistical difference is observed. Therefore post poly-Si nitridation does not cause poly depletion effect under our experimental conditions.

It is observed that combining post poly-Si nitridation with N_2O annealed gate oxide have the best charge-to-breakdown

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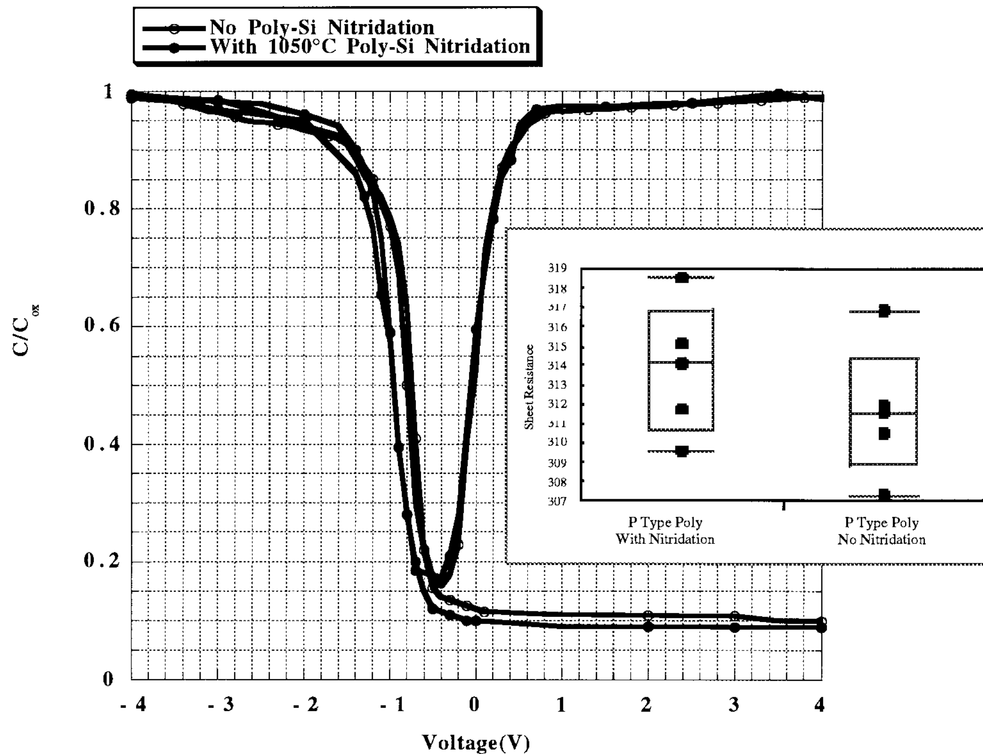

Fig. 1. High (10 kHz) and low (20 Hz) frequency C–V curves for poly-oxide-p substrate capacitors with and without poly-Si nitridation. The insert shows sheet resistance of p type poly-Si with and without NH_3 nitridation..

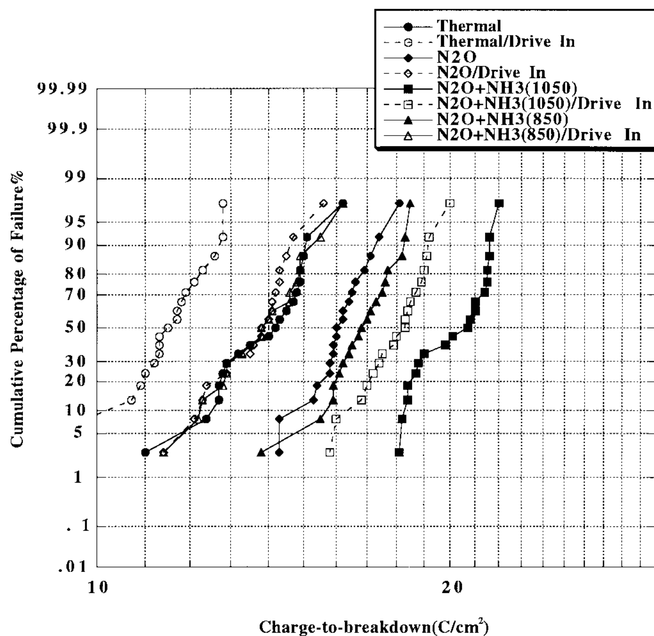

Fig. 2. Q_{bd} of thermal oxide, N_2O annealed oxide, and N_2O annealed oxides with post poly-Si nitridation, before and after boron drive-in.

characteristics, as indicated in Fig. 2. This is due to less boron being able to diffuse into the gate oxide since poly-Si nitridation blocks a fraction of the boron in poly-Si gate from diffusing into the oxide. Figs. 3 and 4 illustrate the SIMS nitrogen profiles for the N_2O annealed gate oxides, with and without poly-Si gate NH_3 nitridation. The oxygen signal at 3100–3200 Å is from the two-step poly-Si deposition process. For N_2O annealed gate oxide, nitrogen concentrates near the SiO_2/Si interface. When the gate poly-Si is annealed in NH_3, net nitrogen concentration increases in the oxide, and has a higher concentration near the poly-Si/SiO_2 interface. The nitrogen concentration at the two-step poly-Si interface provides an additional barrier against boron penetration.

When combining N_2O annealed oxide with poly-Si gate nitridation, the improvement in gate oxide charge-to-breakdown is most significant. This is again illustrated in Fig. 2. Higher post poly-Si nitridation temperature results in higher Q_{bd}. This is due to higher nitrogen incorporation with higher temperature nitridation. It is observed from Fig. 2 that the drive-in process in general causes some additional degradation of gate oxide. It is also observed that even with additional boron drive-in, samples in the 1050 °C nitridation process still exhibit better Q_{bd} than samples with 850 °C post poly-Si nitridation and samples with N_2O annealed oxide only. We believe this is because much less boron is able to diffuse into the gate oxide for oxides with post poly-Si nitridation.

IV. Conclusion

We have demonstrated that by combining N_2O annealed oxide with post poly-Si gate nitridation, oxide reliability is significantly improved. The oxide reliability improvement comes from two factors: 1) intrinsic oxide reliability

TABLE I
EXPERIMENT MATRIX, SHORTHAND NOTATION, AND PARAMETER SHIFT DUE TO 850 °C BORON DRIVE-IN. PARAMETER SHIFT IS NOTED AS NEGLIGIBLE WHEN THERE IS NO SIGNIFICANT STATISTICAL DIFFERENCE BETWEEN THE SPLITS DATA POPULATION

Gate Oxide Type	Post Poly-Si NH_3 Nitridation	850°C Drive-In	Short Hand Notation	ΔV_t(mV)	ΔSS(mV/dec.)	Δg_m(mA/V)
Thermal	No	No	Thermal			
Thermal	No	Yes	Thermal/Drive In	254	156	-0.195
Thermal	Yes(850°C)	No	NH_3(850)			
Thermal	Yes(850°C)	Yes	NH_3(850)/Drive In	223	12.6	-0.145
Thermal	Yes(1050°C)	No	NH_3(1050)			
Thermal	Yes(1050°C)	Yes	NH_3(1050)/Drive In	181	9.7	-0.10
N_2O	No	No	N_2O			
N_2O	No	Yes	N_2O/Drive In	22.4	2.0	Negligible
N_2O	Yes(850°C)	No	N_2O+NH_3(850)			
N_2O	Yes(850°C)	Yes	N_2O+NH_3(850)/Drive In	20.7	0.97(Negligible)	Negligible
N_2O	Yes(1050°C)	No	N_2O+NH_3(1050)			
N_2O	Yes(1050°C)	Yes	N_2O+NH_3(1050)/Drive In	4 (Negligible)	Negligible	Negligible

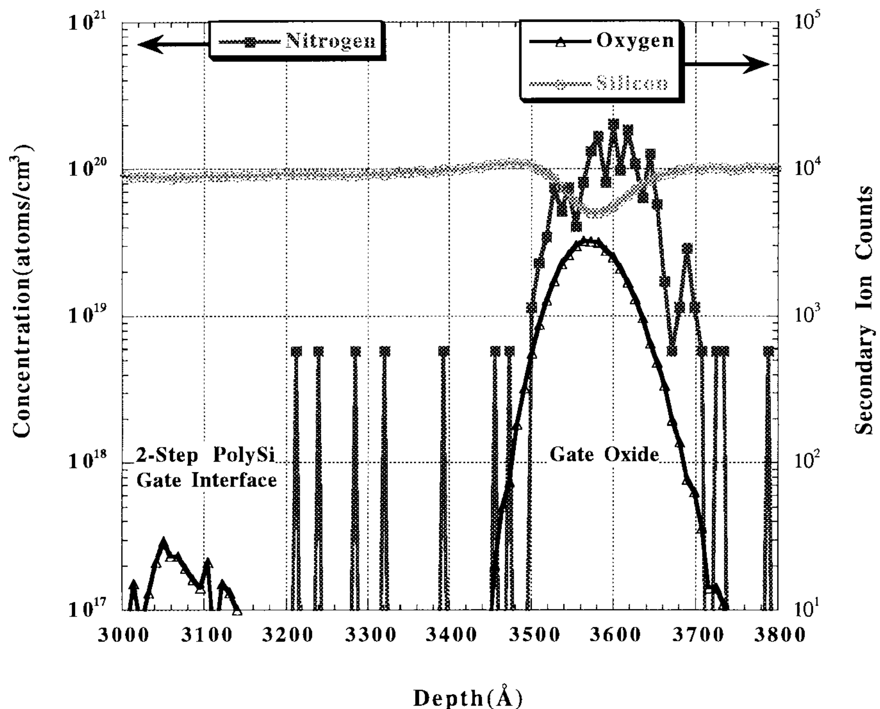

Fig. 3. Secondary ion mass spectrometry nitrogen profiles for N_2O annealed gate oxide.

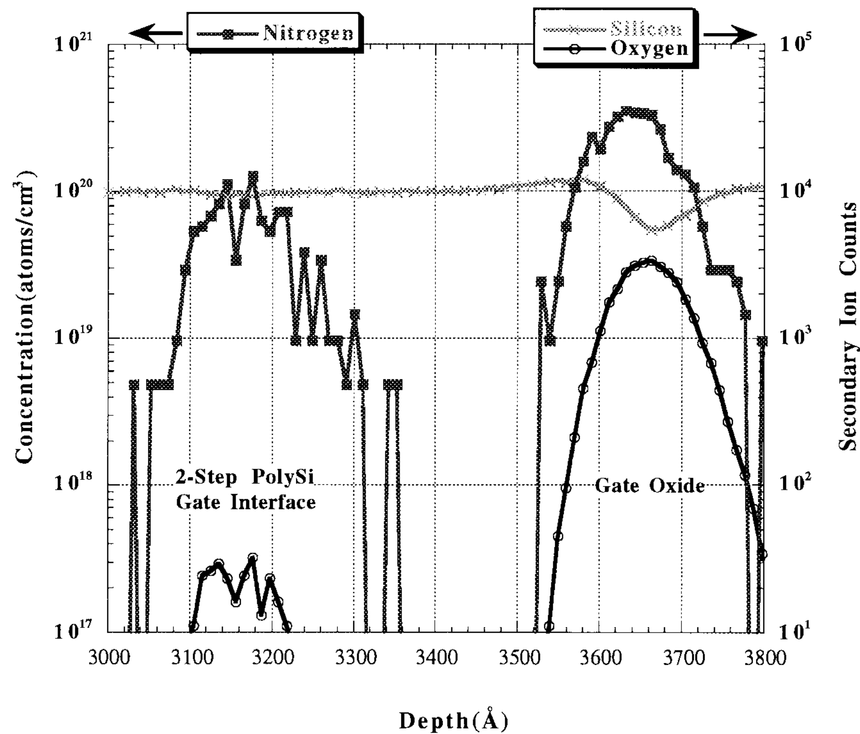

Fig. 4. Secondary ion mass spectrometry nitrogen profiles for N_2O annealed gate oxide with poly-Si gate NH_3 nitridation.

improvement due to nitrogen incorporation near SiO_2/Si substrate interface, and 2) improved immunity against boron penetration into the gate oxide due to post poly-Si nitridation. Post poly-Si gate nitridation reduces the amount of boron able to diffuse into the gate oxide, therefore improves gate oxide reliability against boron penetration. Post poly-Si gate nitridation also incorporates more nitrogen into the gate oxide and improves gate oxide charge-to-breakdown.

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