Leakage Current and Dopant Activation Characterization of SDE/Halo CMOS Junctions with Non-Contact Junction Photo-Voltage Metrology

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Abstract Sheet resistance and leakage current of spike rapid thermal processed (RTP), millisecond flash (fRTP) annealed and chemical vapor deposition (CVD) grown ultra-shallow junctions (USJ) are compared with a non-contact junction photovoltage, RsL, technique. Theoretical reverse-biased diode and non-contact leakage currents are compared. A significant leakage current increase for spike RTP and fRTP processed USJ formed in halo-implanted profiles is described by high electron and hole recombination-generation in the end-of-range (EOR) damage layer enhanced by trap assisted and band-to-band tunneling. The reduced thermal budget of fRTP allows junction formation with reduced dopant diffusion and with lower sheet resistance. However when strong halo doping is employed, there is often a significant increase in junction leakage relative to that for junctions formed in lightly-doped test wafers. This increased leakage current can be reduced by annealing the halo implants before implanting the USJ or by lowering the halo dose. USJ grown with CVD demonstrate low leakage current due to localization of recombination centers at the edge of the depletion layer, where recombination (generation) is small. This study demonstrates the importance of characterizing USJ formed in halo profile for advanced ULSI.

Keywords: Ultra-shallow junctions, junction photo-voltage, sheet resistance, leakage current
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INTRODUCTION

Monitoring of leakage current and sheet resistance of ultra-shallow junctions (USJ) formed in halo profiles or highly-doped epitaxial layers is important for accurate characterization of advanced ULSI technology. However, high junction leakage current density (>10^{-4} A/cm^2) for high sub-junction doping due to band-to-band and trap-assisted tunneling [1,2,3] compromises the measurement of sheet resistance of USJ with contact probes, even when using advanced, non-penetrating four-point probe tools [7]. Non-contact measurements of sheet resistance and leakage current for blanket p-n junctions provides the rapid, accurate characterization required for process control of advanced ULSI technology.

Roger Verkuil developed the first non-contact method and apparatus for the measurement of sheet resistance using junction photo-voltage (JPV) measured with two metal rings placed outside an illuminated area [4]. This approach used an approximate formula for sheet resistance which is valid only for infinitely thin rings and requires that the junction capacitance be known from another technique. This approach does not allow direct measurements of sheet resistance of USJ formed in halo and well profiles.

A rigorous two-dimensional, frequency-dependent JPV method was developed for measurements of sheet resistance and leakage current of USJ formed where the sub-junction doping is determined by local measurements of the junction capacitance [5,6]. Good correlation between this contactless "RsL" technique with "non-penetrating" four-point probes was demonstrated for CVD USJ formed in medium-doped epi layers (7x10^{17} dopants/cm^3), when leakage current due to band-to-band and trap-assisted tunneling is moderate to low (~10^{-7} A/cm^2) [7].

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This paper outlines the theory of RsL leakage current measurements in comparison to reverse-biased diodes and presents experimental results for spike RTP and millisecond-annealed USJs formed in lightly-doped substrates, highly-doped (>10^{18} dopants/cm^3) halo profiles and CVD-grown USJs formed on medium-doped (7×10^{17} dopants/cm^3) epi-layers.

MEASUREMENT BACKGROUND

The basis of the RsL measurement is to use photo-excitation of carriers in a p-n junction and wafer substrate and to monitor, in a spatially resolved manner, the JPV signals inside, V_{in}, and outside, V_{out}, the illumination area, when modulated light produces electron–hole pairs [5,6]. Under illumination, the p-n junction is forward biased (V>0) and the p-n junction voltage at low excitation is $V \ll V_T = kT/q$, where q is the electron charge, k Boltzmann's constant, and T the wafer temperature *(K)*. The junction conductance, $G_{p\text{-}n}$, and leakage current density measured using the RsL method, I_{RsL}, are:

$$G_{p-n} = \left.\frac{dJ}{dV}\right|_{V\to+0} = I_{RsL}/V_T \qquad (1)$$

where $J(V)$ is the p-n junction current density. For an ideal diode:

$$J(V) = I_0[\exp(V/V_T)-1] \qquad (2)$$

where RsL leakage current, I_{RsL}, equals the pre-factor I_0.

By measuring the JPV at the two electrodes at different frequencies, combined with reference JPV measurements on a wafer with a deep p-n junction with known sheet resistance, the sheet resistance, R_s, conductance, $G_{p\text{-}n}$, and capacitance of the p-n junction, $C_{p\text{-}n}$, can be simultaneously determined [5,6].

MODELING OF LEAKAGE CURRENT

We compare the reverse-biased p-n junction leakage current measured by a contact technique with our contactless RsL technique. In our leakage calculations, we do not consider the contribution of reverse-biased diode thermionic current from metal contacts. The p-n junction current density, $J(V)$, is determined by diffusion and recombination (generation) of excess carriers in the bulk, J_{diff}, at the surface, J_S, through recombination (generation) with trap-assisted tunneling (TAT) in the depletion layer, J_{SCR}, and band-to-band tunneling current, J_{BTBT}

$$J(V) = J_{diff} + J_S + J_{SCR} + J_{BTBT} \qquad (3)$$

The recombination (generation) current $J_{SCR}(V)$ is obtained using taking into account trap assisted tunneling [1,2]. Band-to-band tunneling current density in reverse-biased p-n junctions is:

$$J_{BTBT}(V) = cqVE_m^{\sigma}\exp(-E_0/E_m) \qquad (4)$$

where V is the applied junction voltage, E_m the maximum junction electric field and σ a numerical constant (σ = 1 for direct tunneling and σ = 3/2 for phonon-assisted tunneling) [3]. E_0 is a material constant which depends on the effective mass m^* and the semiconductor band gap. The prefactor c depends on the effective mass m^*, the band gap E_g and a factor describing electron-phonon interaction. In our calculations we used $E_o = 1.9\times10^9$ V/m, σ = 3/2, c = 1.6×10^{15}s^{-1} m$^{-1/2}$ V$^{-5/2}$ [3].

In heavily-doped USJ, the contribution of J_{diff} and J_S is small compared to recombination (generation) with trap-assisted tunneling, J_{SCR}, unless the dopants in p-type USJs are not activated and $N_A \ll N_D$ [6]. So we consider only trap-assisted tunneling recombination-generation in the depletion region $J_{SCR}(V)$ and band-to-band tunneling current $J_{BTBT}(V)$. For a non-degenerate n-type halo under forward bias, as in the case of RsL, band-to-band tunneling current is negligible.

The relevant equations for the diode leakage current $I_D(V)$ for $V<0$ and RsL leakage current I_{RsL} for $0<V\ll V_T$ are:

$$I_D(V) = J_{SCR}(V) + cqVE_m^{\sigma}\exp(-E_0/E_m) \qquad (5)$$

$$I_{RsL} = \left.\frac{kT}{q}\frac{dJ_{SCR}(V)}{dV}\right|_{V\to+0} \qquad (6)$$

The recombination profile $U(z, V)$ and leakage currents $I_D(V)$ and I_{RsL} were calculated for an abrupt p-n junction, with junction depth x_j = 10 nm, with a EOR residual damage profile given by:

$$N_t(z) = N_{t\max}\exp\left(-\frac{q(z-z_{\max})^2}{\Delta^2}\right) + N_{tsub} \qquad (7)$$

where N_{tmax} is the peak recombination center concentration at a depth of z_{max} = 20 nm, with a trap distribution width of Δ = 15 nm, recombination cross-sections of $\sigma_n = \sigma_p = 10^{-14}$ cm^2 and trap concentration in the bulk substrate much deeper than z_{max} of $N_{tsub} = 10^{12}$

traps/cm^3. These parameters are descriptive of conditions for shallow junctions formed in implanted halo profiles. For modeling of leakage current for CVD-grown USJ we considered traps to be localized at the interface between the USJ layer and the medium-doped epi-layer with $z_{max} = X_j = 10$ nm , $\Delta = 1$ nm.

With increasing reverse bias, the width and magnitude of the recombination profile U(z,V) increase and the leakage current increases. In the case of low substrate doping concentrations, $N_D = 10^{15}$ dopants/cm^3 ($\rho \sim 10$ Ohm-cm substrate), the depletion region width is about 1 μm and the recombination (generation) profile located in the middle of the depletion region does not overlap the residual damage profile $N_t(z)$ and hence the leakage current is low (Fig. 1).

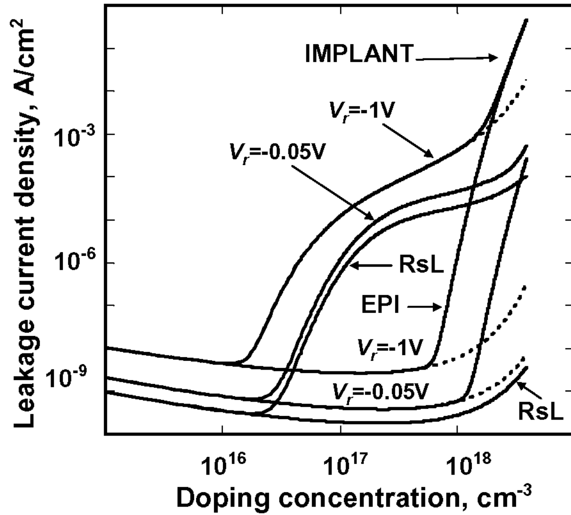

FIGURE 1. RsL and reverse-biased diode leakage current versus substrate doping concentration for implant ($N_{tmax} = 10^{17}$ traps/cm^3) and CVD EPI ($N_{tmax} = 10^{21}$ traps/cm^3) USJ. Dashed curves show the leakage currents without BTBT contribution.

With increasing halo doping concentration, the depletion region width decreases and the recombination profile overlaps the implant residual damage profile leading to a much higher leakage current, as shown in Fig. 1. In the case of CVD-grown USJ, carrier traps are assumed to be localized at the junction growth interface (X_j) and the leakage current is low until TAT and BTBT begin to contribute at $N_D > 10^{18}$ doapnts/cm^3 and the depletion region width shrinks towards W~10 nm. In the case of CVD USJ, BTBT leakage is the dominant factor for $N_D > 10^{18}$ dopants/cm^3.

RsL I_{RsL} and reverse-biased leakage current densities $J_D(V)$ for V_r = -1V, -0.5 V and -0.05V of USJ formed in a halo profile with $N_D = 2\text{x}10^{18}$ doapnts/cm^3 as a function of trap density are shown in Fig. 2. For high reverse bias, the leakage current $I_D(V)$ is significantly higher than I_{RsL} especially for low trap densities where the contribution of BTBT is dominant. Note that for small bias ($|Vr| < 0.05$V) I_{RsL} and $I_D(V)$ are similar.

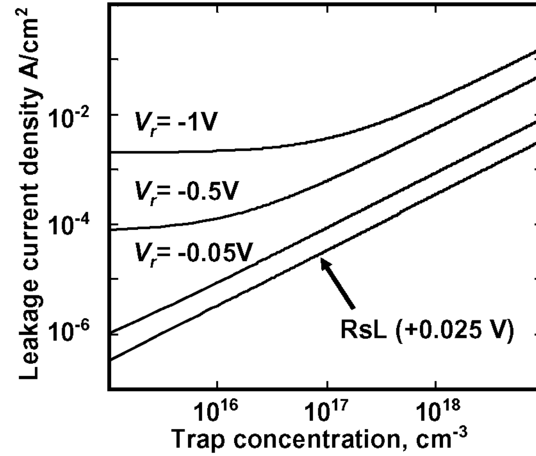

FIGURE 2. RsL and reverse-biased diode leakage current density versus peak trap density for USJ formed in a halo profile ($N_D = 2\text{x}10^{18}$ dopants/cm^3).

EXPERIMENTAL RESULTS AND DISCUSSION

Millisecond anneals were performed using flash-assisted RTP™ (fRTP™), where the wafer is rapidly heated to an intermediate temperature and then its front surface is heated further by a < 1.5 ms pulse of energy from a bank of flash-lamps [8]. Si(100), n-type with $\rho > 2$ Ohm-cm was used. The study included comparisons of 10^{15} B/cm^2 B implants at 500 eV and 5 keV into crystalline and amorphous silicon, the effects of halo doping concentration and the impact of annealing the halo implant before implanting the USJ. The pre-amorphization implants (PAI) were 10^{15} Ge/cm^2 using 30 keV Ge and the halo implants were $4\text{x}10^{13}$ As/cm^2 for 40 keV As. In some samples the halo implants were annealed for 10 s at 1050°C before the PAI or B implants. The final anneals were either a spike anneal at 1050°C or fRTP with preheating to temperatures of 700 or 750°C followed by a pulse to temperatures of T_p = 1250, 1300 or 1350°C. The annealing conditions are summarized in Table 1. Some samples were also processed twice with fRTP recipe D.

Table 1. Anneal conditions.

Spike anneal	1050°C, 100 ppm O_2 in N_2
fRTP A	700°C+DT=600°C(T_p=1300°C)
fRTP B	700°C+DT=550°C(T_p=1250°C)
fRTP C	750°C+DT=600°C(T_p=1350°C)
fRTP D	750°C+DT=550°C(T_p=1300°C)

Low temperature CVD B-doped USJ layers were grown with a junction doping concentration of ~$2x10^{19}$ B/cm^3 on a 20 μm thick medium As-doped ($7x10^{17}$ As/cm^3) epi-layer grown on 10 Ohm-cm n-Si substrates. USJ thickness ranged from 132 nm down to ~2 nm [7].

Figure 3 shows the trends in sheet resistance of USJ with spike and different fRTP conditions for USJ formed in lightly-doped silicon and in pre-annealed halos. These results show consistent improvement of activation, with decreasing sheet resistance, with increasing anneal temperature. Previous studies have shown that fRTP processing of such implants introduces minimal diffusion, hence providing significant benefits compared to traditional spike-annealing approaches [9].

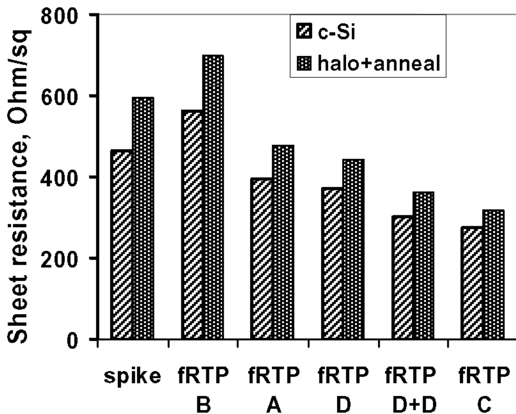

FIGURE 3. Sheet resistance for junctions formed by 500 eV B implants into lightly-doped silicon and pre-annealed halos (halo+anneal) and then annealed by spike RTP or fRTP under different conditions.

Figure 4 shows the junction leakage current trends for several anneal conditions. Spike anneals give consistently low leakage current, regardless of the implant scheme, most likely because dopant diffusion during the spike anneals can drive the junction deeper than the residual implant damage. For sufficiently high peak temperatures, spike annealing can effectively eliminate residual damage [10]. The leakage current density for implants without halo doping was below the measurement limit of 0.1 μA/cm^2, except for the case of fRTP at 1250 C with Ge PAI damage. The presence of halo doping consistently increases the leakage current because of the greatly reduced depletion layer width and overlap of the peak recombination rates with the residual implant damage distribution. Annealing the halo implant damage prior to the B doping steps significantly improved the leakage current. Ge PAI damage resulted in significant leakage current after fRTP anneals at 1250°C, but 1300°C anneals were effective in reducing leakage currents.

These results illustrate that optimization of millisecond annealing demands simultaneous tuning of the halo doping level as well as the thermal annealing process. The reduced thermal budget in the fRTP anneals can leave implant residual defects [11]. The leakage current in halo-doped cases can then be significantly higher than that for spike annealing, even if no leakage degradation is seen in non-halo-doped cases. The halo doping condition must be carefully optimized to take account of this effect. One direct approach is to reduce the halo dose, which should be possible, because the greatly reduced dopant diffusion with fRTP naturally tends to suppress short-channel effects, moderating the need for strong halo doping [12]. Preliminary annealing of halo damage prior to B doping also decreases the leakage current.

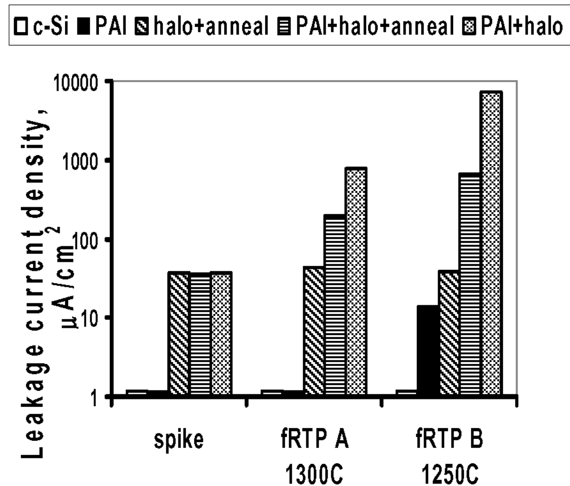

FIGURE 4. Leakage current density from junctions formed by 500 eV B implants into lightly and heavily-doped regions, annealed by various methods.

Figure 5 shows the inverse sheet resistance and junction leakage current versus junction thickness for CVD-grown USJ. The intercept of the 1/Rs trend at ~10 nm indicates that the CVD growth process resulted in an inactive dopant layer of ~10 nm for all layers, corresponding to the high Rs (>10^5 O hm/square) and high leakage current seen for X_j < 10 nm, shown in

Fig. 5 [7]. For the thinnest CVD layers, <10 nm, the lack of p-n junction activity and high leakage current could be due to either structural defects incorporated during the initial stage of the growth process or depletion effects from charged states at the growth interface, or from a combination of these effects.

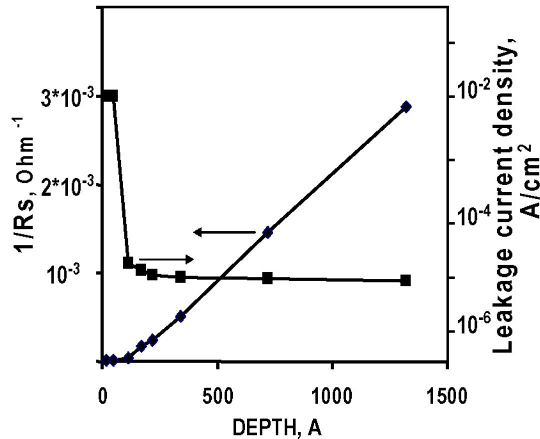

FIGURE 5. Inverse sheet resistance and leakage current density versus layer thickness for CVD USJ.

CONCLUSIONS

Reverse-biased diode and non-contact RsL leakage currents are closely similar for small reverse bias $V< kT/q$. For larger reverse bias, leakage currents are generally higher than RsL leakage measurements due to the added contributions from BTBT and increased TAT tunneling. Significantly higher leakage current levels are observed for USJ formed in highly-doped halo profiles due to high carrier recombination-generation rates increased by trap-assisted tunneling and band-to-band tunneling. The levels of leakage current depend on the process (dopant profiles and activation, location and density of residual damage after annealing) and measurement (sign and magnitude of junction bias) conditions.

Opportunities for process optimization can be seen in the systematic improvements in leakage currents that are observed with RsL measurements for USJ formed in halo profiles where the As implant damage has been reduced by annealing prior to the B doping steps.

Optimization of USJ formation using advanced annealing requires careful balance of halo "strength" and shallow junction doping, balancing control of short-channel effects with leakage current levels. Accurate process monitoring of USJ formed with ms-timescale anneals requires the inclusion of a comprehensive set of interacting implant profiles and thermal processing (halo, PAI, SDE and anneals) in order to provide reliable guidance for process decisions. The challenges posed by the thin (~10 nm) dopant layers and high leakage currents (>10^{-4} A/cm^2), which are characteristic of these combined profiles, rule out the use of contact probes, such as 4-point probes, and favor the use of non-contact measurements of sheet resistance and leakage current, provided by RsL methods. These results show the importance of basing CMOS process choices on accurate, quantitative characterization of dopant activation and leakage currents in multi-profile junctions.

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