Contactless Surface Charge Semiconductor Characterization

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Surface voltage and surface photovoltage have become important semiconductor characterization tools, largely because of their contactless nature and the availability of commercial equipment. The range of the basic technique has been expanded through the addition of corona charge. The combination of surface charge and illumination allows surface voltage, surface barrier height, flatband voltage, oxide thickness, oxide charge density, interface trap density, mobile charge density, oxide integrity, minority carrier diffusion length, generation lifetime, recombination lifetime, and doping density to be determined.

1. Introduction

During charge-based measurements, charge is deposited on the wafer from a corona source, from the ambient, or through a chemical rinse and the semiconductor response is measured. One can drive the charge-oxide-semiconductor (COS) device into deep depletion and measure the recovery transient with a contactless Kelvin probe.[1] It is also possible to bias the COS device into inversion and measure the frequency response by varying the electrical signal applied to the Kelvin probe or by applying a time-varying optical signal to the device.

Kelvin probe measurements, first proposed by Kelvin probe in 1881, are basic to many of these measurements.[2] Kronik and Shapira give an excellent explanation of such probes and their various applications.[3] A *Kelvin probe* is usually operated as a vibrating probe with minimization of the external current. The probes in some charge characterization instruments are not vibrating and we will refer to such probes as *surface voltage probes*. We explain their operation with the aid of Fig. 1. A metal probe, is placed a distance d (typically 0.1 – 1 mm) from the wafer surface. With the work functions of the probe and the semiconductor identical and with no surface charge on the semiconductor surface, the semiconductor bands are flat, as shown by the dashed energy band diagram in Fig. 1(a) and the probe potential, also known as the contact potential difference, V_{cpd}, is zero.

With positive surface charge, the semiconductor is depleted, as shown by the solid energy band diagram in Fig. 1(a). The electrically floating probe will assume a positive contact potential difference equal to the surface potential ϕ_s. With the semiconductor illuminated, the Fermi level splits into two quasi-Fermi levels and both the semiconductor band bending and V_{cpd} are reduced, as illustrated in Fig. 1(b). We will designate the probe voltage with illumination as the surface photovoltage V_{SPV}.

Positive charges, deposited on the semiconductor surface, deplete the surface of the *p*-type sample. Photons, incident on the sample, generate excess carriers within the space-charge region and in the quasi-neutral bulk region. The electrons within the scr and within a distance of approximately the minority carrier diffusion length from the edge of the scr will be collected in the space-charge region and reduce the surface potential barrier. The barrier lowering is similar to a forward-biased junction and the probe detects the difference of the quasi-Fermi levels. For high-level injection, the surface potential vanishes and the probe potential difference between dark and light values is the surface potential.[4]

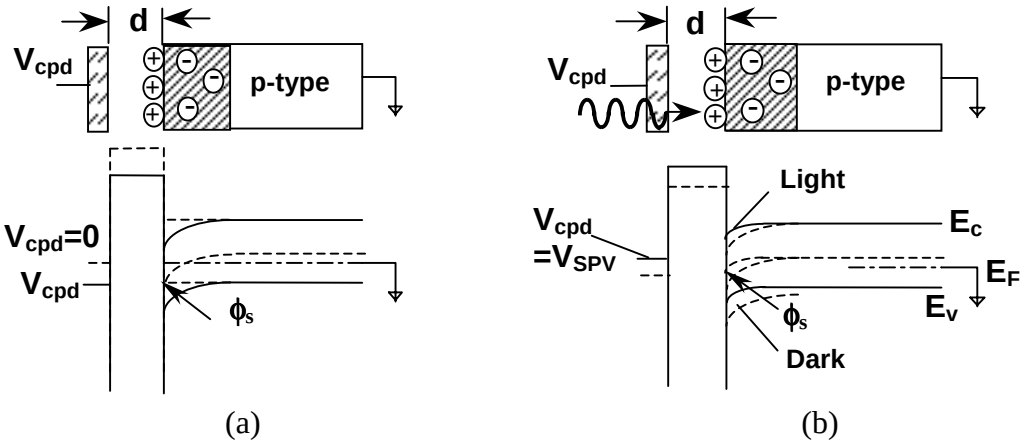

Fig. 1 Surface voltage probe energy band diagram: (a) dark and (b) optical excitation.

2. Corona Charging

Corona charging is a method of depositing charge on a surface, most commonly used in copying processes using xerographic techniques with the charge deposited on the photoconductive drum.[5] One of the first uses in the field of semiconductors was by Williams and Woods[6] and Weinberg[7] to characterize oxide leakage current and mobile charge drift.[8] The method consists of the deposition of ions on a surface at atmospheric pressure through an electric field applied to a source of ions. The corona source consists of a wire, a series of wires, a single point, or multiple points located a few mm or cm above the sample surface.[9]

A potential of 5,000-10,000 V of either polarity is applied to the corona source generating ions close to the electrode. The negative and positive corona ionic species are predominantly CO^{-3} and H_3O^+ (hydrated protons), respectively. The corona source forces a uniform flow of ionized air molecules toward the surface with a few seconds required to charge an insulating surface to a saturation potential. The very short (approximately 0.1 μm) atmospheric mean free path of the ionized gas ensures collision-dominated ion transport with the molecules retaining very little kinetic energy. The charge can be removed with a water rinse.

3. Applications

Minority Carrier Diffusion Length

The minority carrier diffusion length, L_n, is most commonly measured with the surface photovoltage (SPV) technique. In the constant surface photovoltage method, the surface photovoltage, V_{SPV}, is held constant and a series of different wavelengths is selected with each wavelength providing a different absorption coefficient α. The photon flux density Φ is plotted against $1/\alpha$ resulting in a line whose extrapolated intercept on the negative $1/\alpha$ axis is the minority carrier diffusion length. The slope of such a plot contains the surface recombination velocity s_r. In the constant photon flux method, $1/V_{SPV}$ is plotted versus $1/\alpha$.

Iron is one of the most important metallic contaminants with unique properties in *p*-type silicon, forming *Fe-B* pairs in *B*-doped Si. Upon heating at 150-200°C for a few minutes or illumination (20 W/cm^2 halogen light source for about 20 s)[10] the *Fe-B* pairs dissociate into interstitial iron (Fe_i) and substitutional boron (B_s). From the diffusion length before (L_{ni}) and after (L_{nf}) *Fe-B* pair dissociation (see Fig. 2), the iron density N_{Fe} is obtained as[11]

$$N_{Fe} = 1.05x10^{16}\left(\frac{1}{L_{nf}^2} - \frac{1}{L_{ni}^2}\right)\ cm^{-3} \qquad (1)$$

with diffusion lengths in units of μm. This difference in diffusion length between Fe_i and *Fe-B* only obtains at low injection levels and disappears at medium to high injection levels. Metals rarely pair with impurities in n-type Si, although Cu does form such pairs.[12]

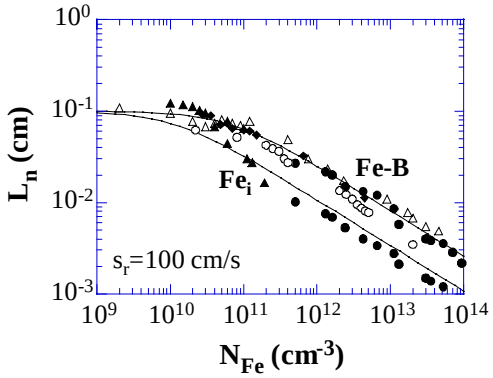

Fig. 2 Effective minority carrier diffusion length for *Fe-B* and Fe_i. The flattening of the data at low iron densities is due to surface recombination. The solid lines are calculated with a surface recombination velocity of 100 cm/s.

Recombination Lifetime

The recombination lifetime is determined through corona charge-based measurements by depositing a sufficient charge to invert the oxidized wafer, forming a zero-biased field-induced *np* junction in a p-type substrate. A brief light flash on the device forward-biases the np junction. After light flash termination, the forward-biased junction returns to equilibrium through electron-hole pair *recombination*. It is this voltage decay that is monitored with a probe. From the time-varying voltage, the recombination lifetime is extracted. This method is analogous to the well-known open-circuit voltage decay technique.[13]

Surface Lifetime

Most SPV measurements are made under dc conditions. However, there is information to be gained by using ac-modulated, low-intensity excitation light. For example, using frequency-modulated light as the excitation source eliminates the need to vibrate the probe. The requirements on the back contact can also be relaxed with a suitable capacitive contact. Consider the sample configuration of Fig. 3. Charge on the surface of the *p*-type wafer induces a space charge of width *W*. Incident light generates electron-hole pairs (ehp) in the sample and the resulting surface photovoltage is measured. For short-wavelength light, most of the electron-hole pairs are generated in the space-charge region.

A convenient way of analyzing the resulting response is through an equivalent circuit. The equivalent circuit concept is very effective in understanding certain concepts of semiconductor device physics and has been used for frequency-dependent optically-induced lifetime measurements by Nakhmanson[14], Kamieniecki,[15] and by Munukata et al.[16] The equivalent circuit consists of the monochromatic, ac-modulated, light-generated photocurrent, the surface charge-induced space-charge region (scr) capacitance, and the various conductances representing the loss mechanisms in the semiconductor due to recombination and generation as illustrated in Fig. 3. Also shown are experimental data and theoretical calculations for a *p*-epitaxial layer on a p^+ substrate. Since blue light leads to ehp generation primarily in the space-charge region, it is the epitaxial layer that is characterized, but the resulting lifetime is

due scr and surface recombination. The best fit between theory and experiment results with a scr recombination lifetime of 1 μs and a surface recombination velocity of 100 cm/s.

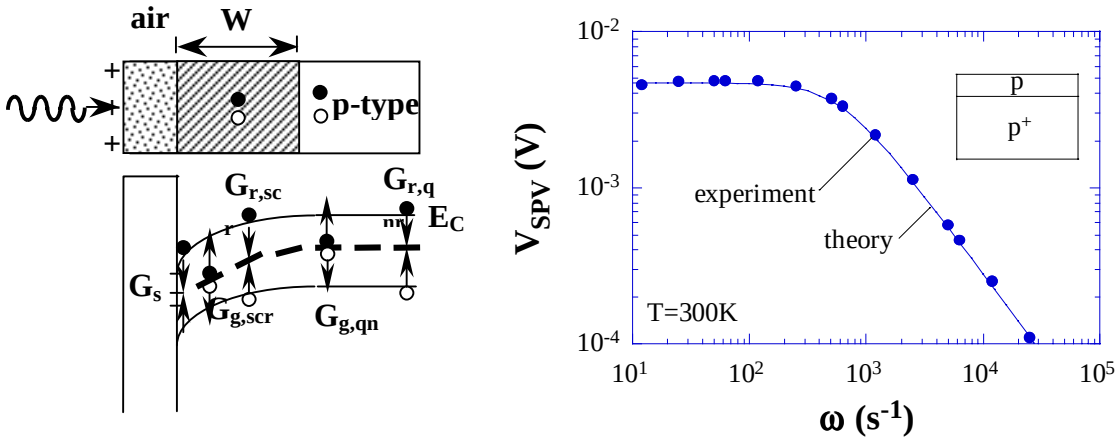

Fig. 3 Sample geometry and conductances due to generation and recombination of excess carriers and experimental/theoretical surface photovoltage data.[17]

In another version of ac SPV, the carrier lifetime is determined from the ratio of the real and imaginary SPV signals.[18] In another commercial version, an oxidized wafer is biased into inversion with pulsed light incident on the sample. Optically generated minority carriers add to the inversion charge, reducing the surface potential and space-charge region width. The measured current I_{signal} contains the relevant parameters.[19] The slope of the I_{signal}/Φ versus Φ plot gives the surface lifetime. The signal also contains the substrate doping density or resistivity.[20]

Generation Lifetime

Generation lifetime measurements are ideally suited for characterization of thin layers, *e.g.*, epitaxial layers, denuded zones, and silicon-on-insulator films, because the characterization depth is the space-charge region width controlled by the applied voltage. A corona charge is pulse-deposited on the oxidized wafer, driving the corona-oxide-semiconductor (COS) device into deep depletion.[21] The device returns to equilibrium through electron-hole pair *generation*. One of the advantages of the COS approach is the constancy of the charge, leading to constant oxide voltage V_{ox} in contrast to conventional MOS-C measurements, where V_{ox} increases as a function of time. This increasing oxide voltage during the capacitance decay limits the voltage that can be applied to a gate because of oxide breakdown or oxide current limitations. It is possible for V_{ox} to become sufficiently high for appreciable oxide or gate current to flow, consisting of electrons injected from the substrate. These electrons originate from the thermally generated inversion layer making it longer to build up the inversion layer. In other words, it will appear as if the generation lifetime is higher than it actually is.[22] No such problem exists in the COS method because the oxide voltage remains constant during the measurement. One simply chooses an oxide voltage for which gate current is negligible.

Charge

The surface voltage dependence on surface charge lends itself to charge measurements (oxide charge, interface trapped charge, plasma damage charge, or other charge). Let us illustrate this by considering mobile oxide charge density Q_m in an oxidized wafer.[23] One way to measure such a charge is to deposit charge on an oxidized semiconductor surface. First de-

posit positive corona charge, then heat the wafer to a moderate temperature of around 200°C for a few minutes, driving the mobile charge to the oxide-semiconductor interface. Cool the sample and determine the flatband voltage V_{FB1}. Next repeat the procedure with a negative corona charge and drive the mobile charge to the oxide-air interface determining V_{FB2}. Q_m is determined by the flatband voltage difference $\Delta V_{FB} = V_{FB2}-V_{FB1}$ through the relation

$$Q_m = C_{ox}\Delta V_{FB} \tag{2}$$

The sensitivity of the measurement can be enhanced by decreasing the oxide capacitance through thicker oxides, but that is inconsistent with today's thin gate oxides. A solution to this problem is to measure the surface potential of an oxidized wafer. Then additional charge is deposited until the surface potential becomes zero. The deposited corona charge is equal in magnitude but opposite in sign to the original oxide charge.[24] The accuracy and precision of this measurement is identical for thin or thick oxides.

Oxide Thickness

Corona charge density Q is deposited on the oxidized wafer and the surface voltage in the dark and under intense light are measured, leading to the surface potential ϕ_s.[25] ϕ_s is then plotted versus deposited charge density as shown in Fig. 4.[26] Such a curve is linear when the device is biased into accumulation or inversion. The oxide thickness is determined from the slope

$$C_{ox} = \frac{dQ}{d\phi_s};\ t_{ox} = \frac{K_{ox}\varepsilon_o}{C_{ox}} \tag{3}$$

This method is not subject to poly-Si gate depletion effects affecting conventional MOS-C measurements,[27] is immune to probe punchthrough and is insensitive to oxide pinhole leakage currents. Repeatability of 0.007 nm has been demonstrated for 1.8 nm thick oxides.[24]

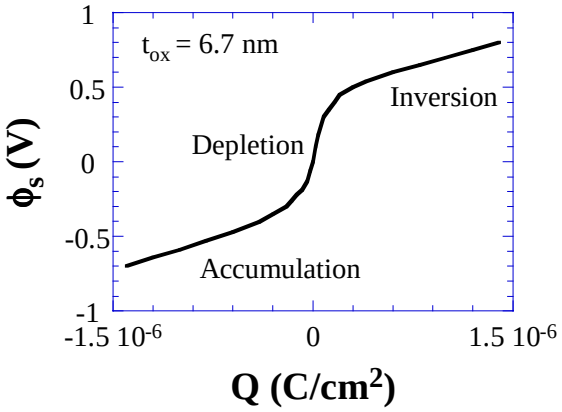

Fig. 4 Surface potential versus surface charge. After Roy et al.[25]

Oxide Leakage Current

To determine oxide leakage current, usually known as gate current in MOS devices, charge is deposited on the surface of an oxidized wafer and the resulting surface voltage is measured as a function of time. The device is biased into accumulation or inversion and the oxide leakage current is determined from the time-varying voltage through the relationship[28]

$$I_{leak} = C_{ox}\frac{dV}{dt} \tag{4}$$

When the charge density is too high, the charge leaks very rapidly through the oxide by Fowler-Nordheim or direct tunneling and the surface voltage is clamped. The deposited charge

density is related to the oxide electric field E_{ox} through the relationship

$$Q = K_{ox}\varepsilon_o E_{ox} = 3.45x10^{-13} E_{ox} \quad (5)$$

for SiO_2. Silicon dioxide breaks down at electric fields of 10-14 MV/cm. For E_{ox} = 12 MV/cm, we find the charge to be $4.1x10^{-6}$ C/cm^2. Fig. 5 is a plot of E_{ox} versus Q clearly showing the electric field saturation at a charge density of around $-4.4x10^{-6}$ C/cm^2.

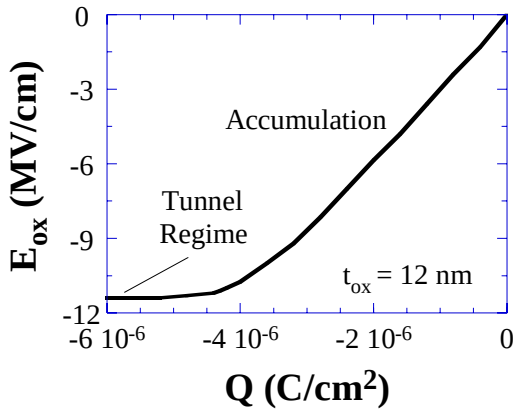

Fig. 5 Oxide electric field versus surface charge for an oxidized wafer. After Roy et al.[25]

4. Summary

Surface voltage and surface photovoltage measurements have become routine in the semiconductor industry. The requisite charge in these measurements is most commonly deposited by rinsing the sample in certain solutions or depositing corona charge. Rinsing is usually done on bare samples and corona charge is deposited on samples covered by insulators. The use of these *contactless* measurement techniques has broadened from initial application of minority carrier diffusion length measurements to a wide variety of semiconductor characterization, including surface voltage, surface barrier height, flatband voltage, oxide thickness, oxide charge density, interface trap density, mobile charge density, oxide integrity, generation lifetime, recombination lifetime, and doping density. It is likely that this range of application will broaden further. As with all characterization techniques, there are limitations but these are frequently less severe than conventional characterization techniques.

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5. References

[1] P. Renaud and A. Walker, *Solid State Technol*. **43**, 143-146, June 2000.
[2] Lord Kelvin, Nature, April 1881; *Phil. Mag*. **46**, 82-121, 1898.
[3] L. Kronik and Y. Shapira, *Surf. Sci. Rep*. **37**, 1-206, Dec. 1999.
[4] E.O. Johnson, *Phys. Rev.* **111**, 153-166, July 1958.
[5] R. M. Shaffert, *Electrophotography*, Wiley, New York, 1975.
[6] R. Williams and M.H. Woods, *J. Appl. Phys*. **44**, 1026-1028, March 1973.
[7] Z.A. Weinberg, *Solid-State Electron.* **20**, 11-18, Jan. 1977.
[8] M.H. Woods and R. Williams, *J. Appl. Phys*. **44**, 5506-5510, Dec. 1973.
[9] R.B. Comizzoli, *J. Electrochem. Soc.* **134**, 424-429, Feb. 1987.

[10] J. Lagowski, P. Edelman, A.M. Kontkiewicz, O. Milic, W. Henley, L. Jastrzebski, and A.M. Hoff, *Appl. Phys. Lett*. **32**, 3043-3045, Nov. 1993.
[11] G. Zoth and W. Bergholz, *J. Appl. Phys.* **67**, 6764-6771, June 1990.
[12] W. Henley, D. Ramappa, and L. Jastrzebski, *Appl. Phys. Lett*. **74**, 278-280, Jan. 1999.
[13] S.R. Lederhandler and L.J. Giacoletto, *Proc. IRE*, **43**, 477-483, April 1955.
[14] R.S. Nakhmanson, *Solid-State Electron*. **18**, 617-626, 1975; *Solid-State Electron*. **18**, 627-634, July/Aug. 1975.
[15] E. Kamieniecki, *J. Appl. Phys*. **54**, 6481-6487, Nov. 1983.
[16] C. Munakata, S. Nishimatsu, N. Homma, and K. Yagi, *Japan. J. Appl. Phys*. **11**, 1451-1461, Nov. 1984; C. Munakata and S. Nishimatsu, *Japan. J. Appl. Phys*. **25**, 807-812, June 1986.
[17] J. E. Park, D. K. Schroder, S. E. Tan, B. D. Choi, M. Fletcher, A. Buczkowski, and F. Kirscht, in *High Purity Silicon VI* (C.L. Claeys, P. Rai-Choudhury, M. Watanabe, P. Stallhofer and H.J. Dawson, eds.) Electrochem. Soc. Proc. **2000-17**, pp 383-395.
[18] E. Kamieniecki, in *Recombination Lifetime Measurements in Silicon* (D.C. Gupta, F.R. Bacher, and W.M. Hughes, eds.), ASTM, **STP 1340**, 147-155, 1998.
[19] S. Liberman, in *Recombination Lifetime Measurements in Silicon* (D.C. Gupta, F.R. Bacher, and W.M. Hughes, eds.), ASTM, **STP 1340**, 156-167, 1998.
[20] P. Roman, J. Staffa, S. Fakhouri, M. Brubaker, J. Ruzyllo, K. Torek, and E. Kamieniecki, *J. Appl. Phys.* **83**, 2297-2300, Feb. 1998.
[21] D.K. Schroder, *IEEE Trans. Electron Dev*. **44**, 160-170, Jan. 1997.
[22] M.Z. Xu, C.H. Tan, Y.D. He, and Y.Y. Wang, *Solid-State Electron.* **38**, 1045-1049, May 1995.
[23] D.K. DeBusk and A.M. Hoff, *Solid State Technol.* **42**, 67-74, April 1999.
[24] S.R. Weinzierl and T.G. Miller, in *Analytical and Diagnostic Techniques for Semiconductor Materials, Devices, and Processes* (B.O. Kolbesen, C. Claeys, P. Stallhofer, F. Tardif, J. Benton, T. Shaffner, D. Schroder, S. Kishino, and P. Rai-Choudhury, eds.), Electrochem. Soc. **ECS 99-16**, 342-350, 1999.
[25] P.K. Roy, C. Chacon, Y. Ma, I.C. Kizilyalli, G.S. Horner, R.L. Verkuil, and T.G. Miller, in *Diagnostic Techniques for Semiconductor Materials and Devices* (P. Rai-Choudhury, J.L. Benton, D.K. Schroder, and T.J. Shaffner, eds.), Electrochem. Soc. **PV97-12**, 280-294, 1997.
[26] T.G. Miller, *Semicond. Int*. **18**, 147-148, 1995.
[27] S.H. Lo, D.A. Buchanan, and Y. Taur, *IBM J. Res. Dev.* **43**, 327-337, May 1999.
[28] Z.A. Weinberg, W.C. Johnson, and M.A. Lampert, *J. Appl. Phys.* **47**, 248-255, Jan. 1976.