MERCURY PSEUDO-MOSFET (HgFET) DRAIN CURRENT DEPENDENCE ON SURFACE TREATMENT

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The effects of surface treatment by a dilute HF rinse on the drain current – gate voltage characteristics in HgFETs have been investigated by experimental measurements and numerical simulations. The apparent threshold voltage increases and interface trap density decreases with time after the HF rinse is due to a coupling between the Si film/BOX interface and the positively charged, hydrogen-terminated surface acting as a back gate in the thin-film fully depleted HgFET.

INTRODUCTION

The pseudo MOSFET is a simple, yet powerful, device to characterize various aspects of SOI wafers [1,2] and is routinely used for incoming wafer inspection to determine several material parameters [3]. It comes in the point contact and the mercury probe (HgFET) configurations. The HgFET has the advantage of well-defined source/drain contacts, but it has an Hg/Si interface and all the vagaries that accompany metal/Si contacts. In a previous study [4], we observed that the Hg/Si barrier height changes with time after dilute HF/H_2O, 1:20 rinse, that is essential to reduce the barrier height for n-channel devices. Si surfaces, prepared in HF-containing solutions, are completely H-terminated and remarkably passive [5]. This is somewhat surprising since thermodynamics suggests there should be significant Si-F bonds (Si-F and Si-H bond energies are 6.2 and 3.3 eV). However, if one considers the complete system formed by reactants, reaction products and the surface, hydrogen termination is thermodynamically favored compared to fluorine termination.

The HF rinse terminates dangling bonds at the Si surface, reducing surface states and deposits positively charged hydrogen ions [6]. The hydrogen-terminated Si surface, however, oxidizes when exposed to air and the surface charges are dissipated and surface states appear to increase [7]. Fermi level pinning has also been attributed to HF-treated Si surfaces [8].Hovel represents the surface states as back surface (Si/air) interface states (D_{it2}) to be considered when the threshold voltage and front surface (Si film/BOX) interface states (D_{it1}) are determined [2]. More recently, an HF-induced surface channel in a pseudo-MOSFET was observed immediately after HF rinse [9].

In this paper, we show that a dilute HF rinse impacts the HgFET drain current by changing the barrier height at the Hg/Si interface and by forming a parasitic channel at the Si film surface. This electro-chemically changed surface induces coupling between the top surface and the Si/BOX interface in the subthreshold regime, similar to fully depleted SOI MOSFETs with positive back gate bias. These HF-induced effects depend on time after HF rinse, presumably because an oxide grows on the Si surface. We also used 2-D device simulation to support our explanation.

EXPERIMENT

We used SIMOX wafers with Si film and buried oxide (BOX) thicknesses of 190 nm and 390 nm. The wafers are etched into islands to reduce leakage currents around the edge of the wafer and through BOX defects. The Four Dimensions CV Map 92-B, a commercial Hg-contact probe system, is used for current-voltage measurements. Source and drain are formed by Hg pressure using a recycling Hg flow through the probe contacts to provide continuous cleaning of the Hg. The mercury probe is made up of a central circular source and a horseshoe-shaped drain, shown in Fig. 1. The Hg probe contacts the sample facing down, while the wafer back is contacted by a metal chuck. The Hg probe is lifted after each measurement and the wafer rests on the probe station in room ambient between measurements.

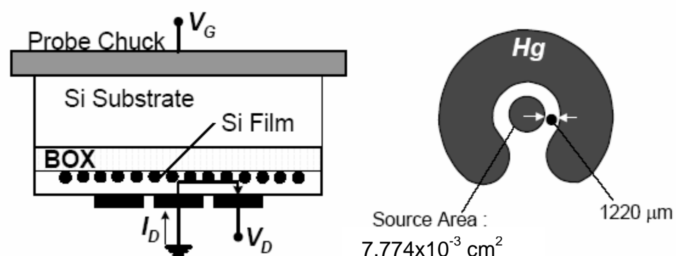

Figure 1. HgFET and the Hg probe geometry.

The wafers are etched for 1 min in HF/H_2O, 1:20 followed by a DI water rinse and N_2 gas dry and the first I_D-V_G measurement is made approximately 10 min after the rinse. The dilute HF rinse is essential for maximum electron drain current. We measured the curves repeatedly up to 195 h after the rinse. Some samples are further annealed in forming gas at 450°C for 30 min to reduce interface traps at the Si/BOX interface.

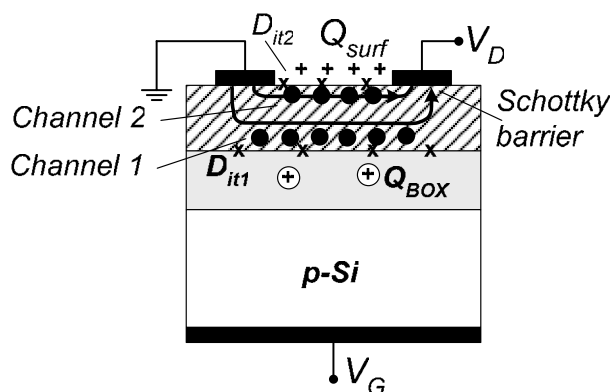

Figure 2. *n*-HgFET cross-section showing the parasitic electron path from source to drain (channel 2) induced by the surface charge Q_{surf} after HF rinse. Also shown are D_{it1} at the Si/BOX interface and D_{it2} at the surface.

We show in Fig. 2 an *n*-HgFET biased into inversion by a positive gate voltage. Immediately after HF rinse, there is a positive surface charge, Q_{surf}, inducing weak electron channel 2 at the upper Si surface. This channel cannot be turned off with the gate voltage,

but disappears in time as the surface charge dissipates. Electrons in the main channel (channel 1) at the Si/BOX interface face several impediments on their way from source to drain. They must overcome the Schottky barrier at the source, the depleted region from source to channel, the depleted region from channel to drain, and the drain Schottky barrier.

Representative I_D-V_G curves are shown in Fig. 3, where immediately after the HF rinse ($t = 0^+$), the electron drain current ($+V_G$) is highest and the hole drain current ($-V_G$) is lowest. We believe this is due to the low Hg/Si barrier height for electrons and high barrier height for holes. With time, the barrier heights change, the electron drain current decreases and its threshold voltage increases, while the hole drain current increases and its threshold voltage also increases. This behavior with time is reproducible after repeated dilute HF rinses. The minimum I_D (initially at $V_G \approx$ -3 V) gradually decreases with time, which we believe is caused by Q_{surf} dissipation, leading to disappearance of channel 2. The drain current decrease at V_G = 5-10 V we believe is caused by an increasing electron barrier height at the Hg/Si interface.

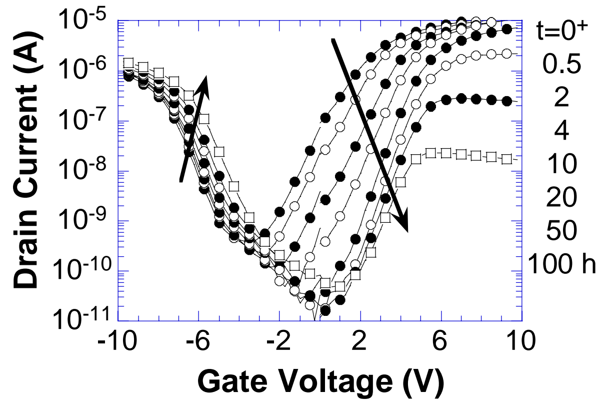

Figure 3. Drain current versus gate voltage as a function of time following dilute HF rinse. SIMOX, t_{Si}=190 nm, t_{BOX}=390 nm.

How does the threshold voltage change with time? The gate voltage for a fully depleted film with a depleted or inverted top surface is given by [2]

$$V_G = \phi_{MS} - \frac{Q_{BOX}}{C_{BOX}} + \left(1 + \frac{C_{it1} + C_{it2}/(1+R)}{C_{BOX}}\right)\phi_s - \frac{Q_{surf} + Q_{s,2}}{C_{Box}(1+R)} - \frac{Q_{s,1}}{C_{BOX}} + \frac{Q_{Si}}{2C_{BOX}}\left(1 + \frac{1}{1+R}\right) \quad (1)$$

where ϕ_{MS} is the gate/semiconductor work function difference, Q_{BOX} contains all charges in the BOX assumed to be at Si/BOX interface in the BOX, Q_{surf} is the charge density on the Si film surface, $Q_{s,2}$ the mobile charge density in the Si film at the surface (channel 2), $Q_{s,1}$ the mobile charge density at the Si film/BOX interface (channel 1), $C_{it1} = qD_{it1}$ and $C_{it2} = qD_{it2}$ the interface trap capacitances at the bottom and top Si layer surfaces, $Q_{Si} = qN_At_{Si}$ is the depletion charge in the Si film, and $R = C_{it2}/C_{Si}$. With the doping density in the gate equal to that in the Si film, $\phi_{MS} = 0$. We further assume that at threshold $Q_{s,1} \approx 0$ and $\phi_s = 2\phi_F$. With these considerations, the threshold voltage is

$$V_T = -\frac{Q_{BOX}}{C_{BOX}} + \left(1 + \frac{C_{it1} + C_{it2}/(1+R)}{C_{BOX}}\right)2\phi_F - \frac{Q_{surf} + Q_{s2}}{C_{Box}(1+R)} + \frac{Q_{Si}}{2C_{BOX}}\left(1 + \frac{1}{1+R}\right) \quad (2)$$

We further assume that the HF rinse induced surface charge density on the sample induces an equal charge density in the Si film, *i.e.*, $Q_{surf} = -Q_{s,2}$, leaving C_{it2} as the only variable in Eq. (2). D_{it2} varies from a very low density due to passivation of Si dangling bonds immediately after the HF rinse to a higher density due to native oxide growth with time while D_{it1} remains constant unless Si/BOX interface properties are altered by other means, *e.g.,* voltage stress or high energy radiation. In the simulation, we assume D_{it1} = 1.5x10^{11} cm^{-2}eV^{-1}, a typical value for SIMOX wafers. Equation (2) is plotted in Fig. 4 as a function of D_{it2}.

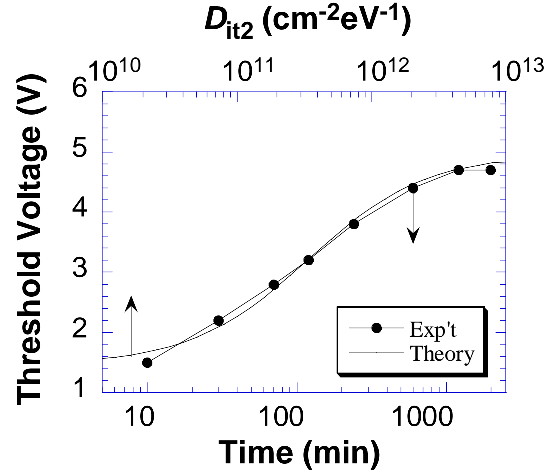

Figure 4. Threshold voltage versus surface state density D_{it2} at the Si surface and versus time. Theory: t_{Si} = 190 nm, t_{BOX} = 390 nm, $N_A = 10^{15}$ cm^{-3}, D_{it1} = 1.5x10^{11} cm^{-2}eV^{-1}, Q_{BOX}/q = 6x10^{10} cm^{-2}; experimental data from Fig. 3.

The threshold voltage is straightforward to determine for the higher drain currents, by linear extrapolation, for example [10]. However, as the drain current decreases with time, the linear extrapolation method no longer works, because the current is too low. Hence we limit the threshold voltage determination from the data in Fig. 3 to 40 h and plot these also in Fig. 4. The theoretical curve agrees well with experimental data, confirming that the top surface states are the likely cause of the threshold voltage shift. From Eq. (3) we find that the surface state density increases from ~ 10^{10} cm^{-2}eV^{-1} immediately after HF rinse to about 5x10^{12} cm^{-2}eV^{-1} after an oxide forms.

In addition to the threshold voltage shift, it is worth noting that the subthreshold slope in Fig. 2 changes with time even though nothing is done to alter the Si/BOX interface properties. We do not believe that the HF rinse affects the Si/BOX interface. Although it is possible for hydrogen to diffuse through the thin Si film to the Si/BOX interface in the many hours in Fig. 3, the drain current returns to its initial value immediately upon a second HF rinse with insufficient time for hydrogen diffusion. The interface trap density is extracted from the subthreshold slope given by [2]

$$S \approx \ln(10)\left(\frac{q}{kT} - \frac{1}{E_F t_{Si}}\right)^{-1} \frac{C_{ox} + C_{it1} + C_{Si}}{C_{BOX}} \tag{3}$$

where E_F is the electric field at Si film/BOX interface. Using Eq. (3), the interface trap density D_{it1} with time is calculated from the subthreshold slope in Fig. 2 and shown in

Fig. 5 for a conventional, unannealed wafer and one annealed in forming gas at 450°C for 30 min. As expected, the forming gas anneal reduces the interface trap density, D_{it1} at the Si/BOX interface due to hydrogen diffusing through the Si film to passivate dangling bonds at the Si film/BOX interface. However, merely exposing the HF-rinsed sample to air appears to reduce D_{it1} for both samples in Fig. 5.

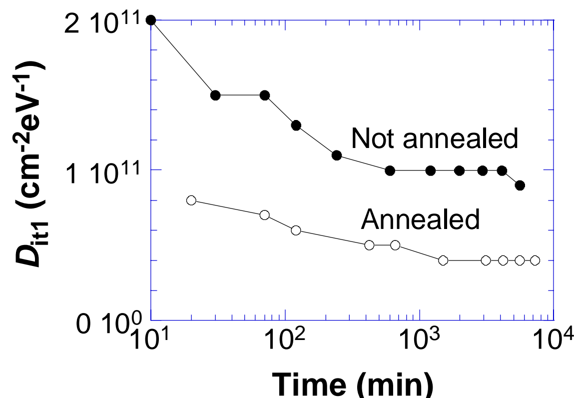

Figure 5. Interface trap density versus time for non-annealed and forming gas (450°C/30 min) annealed wafers. SIMOX, t_{Si}=190 nm, t_{BOX}=390 nm.

This behavior cannot be explained by the conventional pseudo-MOSFET theory [2] which predicts increasing interface density up to the time when C_{it2} becomes much larger than C_{si}. Hereby, we introduce the coupling effect deduced from a fully depleted SOI *n*-MOSFET with back gate under positive bias. Wouters, et al. [11] suggested that back-channel conduction in SOI MOSFETs dominates when the back-surface (Si film/BOX) potential is higher than the front-surface (Si film/gate oxide) potential. Consequently, the subthreshold slope degrades as C_{it2} increases. This suggestion is well adapted to our case where the HgFET positive surface charge is similar to back bias in a conventional SOI MOSFET. The upper surface is strongly charged immediately after the HF rinse, resulting in a higher surface potential than at the Si film/BOX interface to induce channel 2 (Fig. 1). As the surface charge dissipates, the upper surface potential weakens, the surface potential at the Si/BOX interface becomes dominant and finally only channel 1 exists. Equation (3) applies when the upper surface is either depleted or accumulated.

SIMULATIONS

Interface trap density and threshold voltage are calculated with SILVACO Atlas for the same configuration as our experimental devices. As mentioned previously a dilute HF rinse does not only induce a positive surface charge but also decreases the Hg/Si Schottky barrier height. The positive surface charge dissipates with time while the Schottky barrier height increases. In the simulations we vary the positive surface charge from $5\text{x}10^{12}$ to $5\text{x}10^{9}$ cm^{-2} and the corresponding Hg/Si barrier height from 0.44 to 0.6 eV. The experimental interface trap density versus time after HF rinse and the simulated D_{it2} versus barrier height are shown in Fig. 6.

Although the simulated interface trap density is plotted as a function of Schottky barrier height, it assumes different surface charge densities in the range of $5\text{x}10^{12}$ to $5\text{x}10^{9}$ cm^{-2}. Even though there is some discrepancy between simulation and experimental data,

the trend is the same As a result of simulation and experiment, we propose that positive surface charge from the HF rinse forms a parasitic surface electron channel at the top surface of the Si film immediately after HF rinse and gives a low barrier height, inducing a coupling between the upper Si film surface and Si film/BOX interface similar to a fully depleted SOI MOSFET.

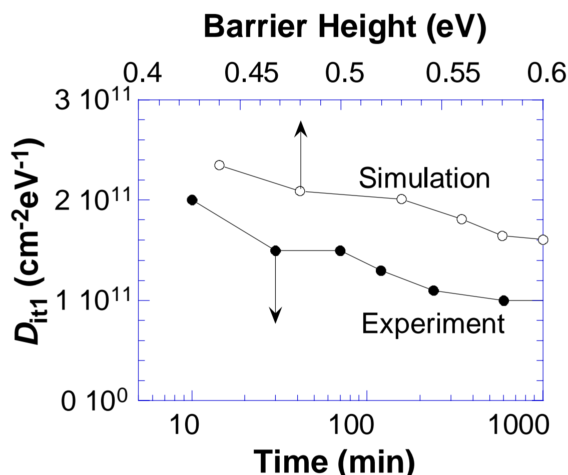

Figure 6. Simulated interface trap density versus Hg/Si barrier height, and experimental interface trap density versus time; $t_{Si} = 190$ nm, $t_{BOX} = 390$ nm, $N_A = 10^{15}$ cm^{-3}; experimental data from Fig. 3.

CONCLUSIONS

We have presented evidence of drain current dependence on surface states/charge after a dilute HF rinse through HgFET current-voltage measurements as well as device simulations. A dilute HF rinse does not only reduce the Hg/Si Schottky barrier height, but also induces positive surface charge on the Si film surface and reduces surface states due to hydrogenation of Si dangling bonds. The threshold voltage shifts to negative voltage and the interface trap density at the Si/BOX interface determined from the subthreshold slope appears to increase due to the positive surface charge immediately after the HF rinse. After HF rinse, the threshold voltage shifts positively and the interface trap density decreases with time after exposure to air. We believe that the coupling between the Si film surface and Si film/BOX interface, similar to a fully depleted SOI *n*-MOSFET with back bias, leads to the drain current dependence on surface states/charge. Hence it is important that extraction of threshold voltage and Si/BOX interface trap density be done carefully in HgFETs.

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