Low Power Silicon Devices

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Introduction

Low power electronics had its beginnings in 1947 when the transistor was invented and replaced power-hungry vacuum tubes. Until the invention of the silicon integrated circuit in 1958, however, semiconductor devices existed as discrete devices and circuits were not particularly low in power consumption compared to today's circuits, but much lower than vacuum tube circuits. Integrated circuits (ICs) reduced power consumption further, because numerous devices could be placed on one chip, alleviating the interconnect problem and reducing power consumption. However, the key low-power breakthrough was the invention of the complementary metal-oxide-semiconductor (CMOS) integrated circuit in 1963.[1] Most integrated circuits, especially low-power ICs, use CMOS devices as their building blocks.[2]

The need for low power electronics is driven by three distinct applications: 1. portable electronic products, such as hearing aids, cardiac pacemakers, wrist watches, pocket calculators, personal digital assistants, etc., 2. continually increasing packing density of devices on integrated circuits for enhanced performance imposing stringent restrictions on power dissipation, and 3. conservation of power in desktop systems where a competitive life cycle cost-to-performance ratio demands low power for reduced power supply and cooling costs.[3] Lower power consumption leads to reduced chip temperatures and higher reliability and allows less expensive plastic packages.

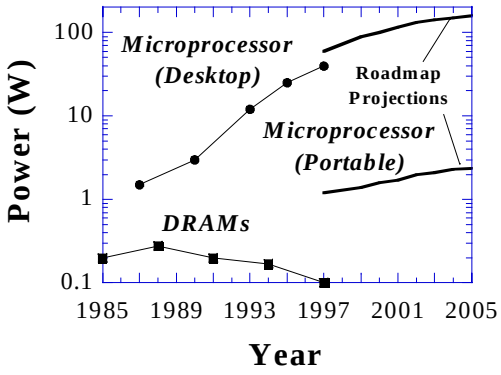


Fig. 1 Actual and projected power dissipation versus year of production for (a) microprocessors, (b) DRAMs.

Experimental[4] and projected[5] power dissipation data for microprocessors and for dynamic random access memories (DRAMs)[6] are shown in Fig. 1. For desktop applications, the power dissipation is approaching 100 W per chip and is projected to exceed that value. There is a very large power dissipation difference between desktop applications where cooling fans are permissible and portable electronics where cooling in the unit is more difficult and batteries have limited lifetime. DRAM circuits have significantly lower power consumption. Power dissipation issues in electronic systems are addressed at various levels. Of the various hierarchies in electronic systems (materials, devices, circuits, and systems), we address device issues here as they relate to low power electronics.

Device Background

Integrated circuits come in two basic implementations: digital and analog circuits. A digital circuit consists of a series of switches and storage capacitors that store "ones" and "zeros". A simple representation of a digital switch and its associated access line is shown in Fig. 2, where neither the line nor the switch are ideal. For a transistor to change its state from a "one" to a "zero" or a "zero" to a "one", the signal must first reach the device by traveling along the access line and then the device must switch. A voltage pulse, applied at the input terminal, is delayed before it reaches the switch. The delay time is determined by series resistance R_s and parallel capacitance C_p. Short delay times demand low R_s and low C_p.

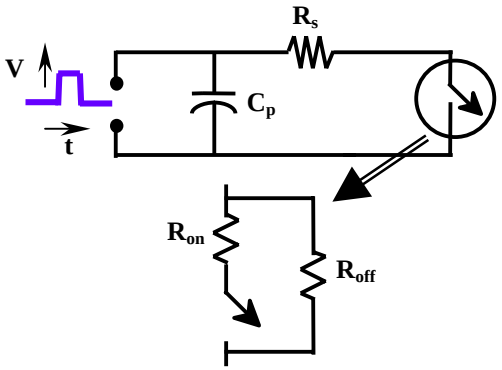


Fig. 2 A digital switch consisting of the access line resistance R_s and capacitance C_p, and switch resistances R_{on} and R_{off}.

The Encyclopedia of Materials: Science and Technology (K.H.J. Buschow, R.W. Cahn, M.C. Flemings. B. Ilschner, E.J. Kramer, and S. Mahajan, eds.), Elsevier, 2001.

The low resistance is achieved through appropriate metallic films on the IC with copper being the preferred material because, other than silver, it has the lowest resistance of any metal. The capacitance issue is addressed through the use of insulators with lower dielectric constants than silicon dioxide, the material of choice in the past. The switch has non-zero "on" resistance, R_{on}, when it is closed and finite "off" resistance, R_{off}, when it is open. This has important implications for low power operation, because R_{on} leads to power dissipation in the "on" state and R_{off} to power dissipation in the "off" state.

To understand low power electronics, it is necessary to understand the building blocks of integrated circuits - the semiconductor devices. Low power circuits consist of complementary metal-oxide-semiconductor devices. The building block of CMOS is the metal-oxide-semiconductor field-effect transistor (MOSFET), illustrated in Fig. 3. It consists of a p-type silicon (Si) wafer (the substrate or body, B). The "p" means it is doped with acceptor-type impurity atoms (e.g., boron) making the substrate p-type, i.e., conduction takes place by positively-charged holes. Two n-type regions are formed in the substrate. The "n" means these regions are doped with donor-type impurity atoms (e.g., arsenic or phosphorus) making them n-type, with conduction by negatively-charged electrons. One n-region is the source (S) and the other is the drain (D). The source and drain np junctions are also known as diodes. The region between the two diodes is covered by the gate oxide, which in turn is covered by a conducting material, the gate (G).

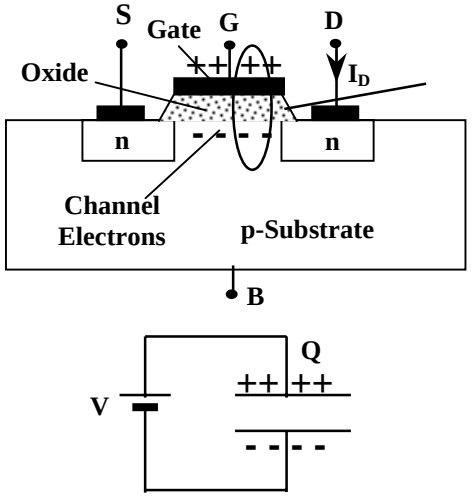


Fig. 3 A schematic MOSFET and its equivalent capacitor representation.

The gate was originally a metal but today it is most commonly made of heavily-doped polycrystalline Si. A positive gate voltage induces electrons in the channel - the region between source and drain - and these electrons flow from source to drain in response to a positive drain voltage. This type of MOSFET is known as an *n-channel* device because the channel consists of negatively-charged electrons. In a *p-channel* MOSFET, the substrate is n-type and the source and drain are p-type and the channel consists of holes. Voltage polarities are reversed in p-channel devices compared with n-channel devices, i.e., the gate and drain voltages are negative to turn the device on.

The gate-oxide-semiconductor portion of the device, indicated as "capacitor", can be viewed as two plates separated by the oxide thickness, also shown in Fig. 3. When a voltage is applied to a capacitor, positive charge is deposited on the capacitor plate near the positive power supply terminal and negative charge on the other plate. A MOSFET can be viewed as a capacitor containing diodes at both ends of the lower plate. In its simplest mode, an n-channel MOSFET operates by applying a positive gate voltage and a positive drain voltage. The positive gate voltage leads to positive gate charge and negative semiconductor charge. The negative semiconductor charge in the channel consists of electrons. A positive drain voltage causes the channel electrons to flow from the source to the drain, leading to a drain current, I_D, in the opposite direction due to the negative electron charge. For zero gate voltage, the drain current is ideally zero and for positive gate voltage above the threshold voltage, drain current flows. The device is not ideal, however, and some of these non-idealities are important for low-power applications.

MOSFET Current-Voltage Characteristics

To understand MOSFETs, it is necessary to understand their current - voltage characteristics. The simplest equations that illustrate this behavior and are very useful for low power considerations will be used. The drain current (I_D) - drain voltage (V_D) relationship can be expressed by the equation

$$I_D = \frac{W\mu C_{ox}}{L}\left(V_G - V_T - 0.5V_D\right)V_D \qquad (1)$$

where W is the gate width, L the gate length, μ the mobility of the electrons in the channel, C_{ox} the oxide capacitance/unit area, V_G the gate voltage, and V_T the threshold voltage. The gate voltage at which appreciable drain current starts to flow is the threshold voltage. I_D – V_D curves are shown in Fig. 4. The two most critical

dimensions of a MOSFET are its gate length, often called the channel length, and gate oxide thickness. They vary widely, but gate lengths are typically (0.2-5)x10^{-4} cm and oxide thicknesses (2-10)x10^{-7} cm.

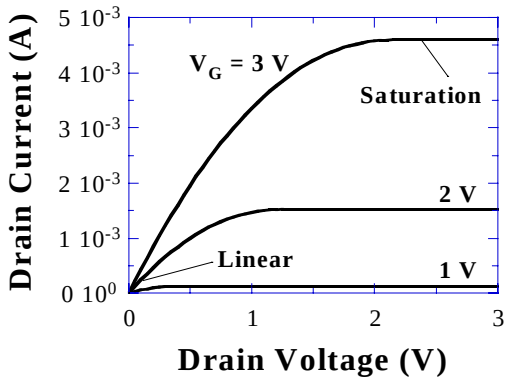


Fig. 4 MOSFET drain current - drain voltage characteristics.

The drain current rises linearly at low drain voltages and eventually saturates. In saturation, the drain current becomes

$$I_{Dsat} = I_{on} = \frac{W\mu C_{ox}}{2L}(V_G - V_T)^2 \qquad (2)$$

This saturation current is referred to as the "*on*" current. When semiconductor devices are used as switches in digital circuits, they usually operate either at zero gate voltage or in saturation with gate and drain connected to each other and Eqn. (2) is the relevant equation. Increased gate voltages lead to higher drain currents, because the channel contains more electrons. The goal of a switching circuit is to have the "on" current as high as possible for lowest switching time.

Equations (1) and (2) only hold for gate voltages above the threshold voltage. For $V_G < V_T$, the drain current is related to the gate voltage by

$$I_D = I_T \exp[q(V_G - V_T)/nkT] \qquad (3)$$

where I_T is the threshold current, i.e. the drain current at $V_G = V_T$, q is the charge of an electron (1.6x10^{-19} C), k is Boltzmann's constant (1.38x10^{-23} J/K), T the temperature (in K), and n is a factor that depends primarily on the doping density of the substrate. Typical values of n are around 1.5 and I_T is frequently taken to be 10^{-6} A. At $V_G = 0$, the drain current is given by

$$I_D = I_{off} = I_T \exp(-qV_T/nkT) \qquad (4)$$

The "off" current is the current that flows through the MOSFET when it is "off" or when the gate voltage is zero. This current becomes an important low power consideration, because it represents a drain on the power supply when the devices are "off". Equations (2) and (4) illustrate the importance of the threshold voltage. It appears in both "on" and "off" current expressions. The goal of a switching circuit is for the "off" current to be as low as possible and for the "on" current to be as high as possible.

An important parameter of a switch (MOSFET) is the voltage (gate voltage) necessary to change the current (drain current) from its "off" current to its "on" current. The most common designator for this is the *subthreshold swing* S, defined as the gate voltage necessary to change the drain current by one decade, i.e., by a factor of ten. From Eqn. (3),

$$S = \frac{dV_G}{d\log(I_D)} = \frac{\ln(10)nkT}{q} = 0.2nT \ mV/decade \qquad (5)$$

With n ≈ 1.5, this leads to about S ≈ 90 mV/decade and 125 mV/decade at 25°C and at 150°C, respectively.

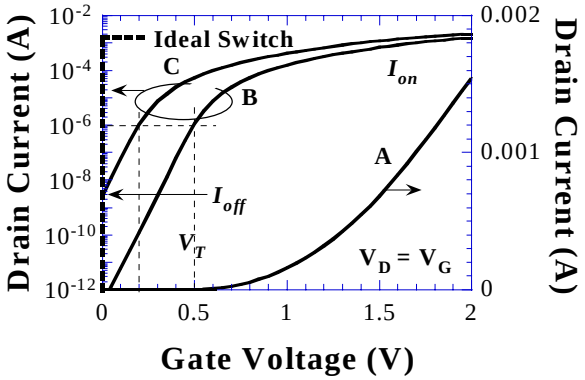


Fig. 5 MOSFET drain current - gate voltage characteristics shown both as semilog and linear plots.

The threshold voltage is shown on a plot of drain current versus gate voltage in Fig. 5. The "Ideal Switch" line represents the current - voltage behavior of an ideal switch. When it is "off", the current is zero and when it is "on", there is negligible voltage drop across such a switch. A MOSFET is a non-ideal switch. When it is "off", there is a small leakage current flowing through the device and when it is "on" there is a voltage drop across the device, illustrated by R_{on} and R_{off} in Fig. 2. Although the "off" current may be quite low, when multiplied by all the devices on a chip, which may be

hundreds of millions of devices, the power dissipation can become significant. For example, for a circuit with 10^9 devices, the total "off" current is 0.1 A for $I_{off} = 10^{-10}$ A for each device.

Curve "A" in Fig. 5 is a linear I_D - V_G plot, showing the drain current to be very low at gate voltages below about 0.5 V. The same curve, plotted on a semilog plot as "B", shows there to be drain current all the way to zero gate voltage. The threshold voltage is here defined as that gate voltage corresponding to a drain current of 10^{-6} A. The threshold voltage is 0.5 V for curves "A" and "B". The threshold voltage is reduced to 0.2 V for curve "C". Curves "B" and "C" illustrate a very important aspect of MOSFET switches. As the threshold voltage is reduced, the "on" current increase (desirable) is moderate, but the "off" current increase (undesirable) is significant. The "off" current changes much more with threshold voltage than does the "on" current. The relationship between "off" and "on" currents is illustrated in Fig. 6. This figure clearly shows the trade-off between the two currents; high "on" current also implies high "off" current.

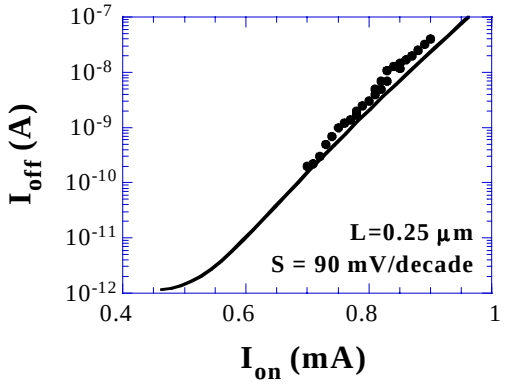
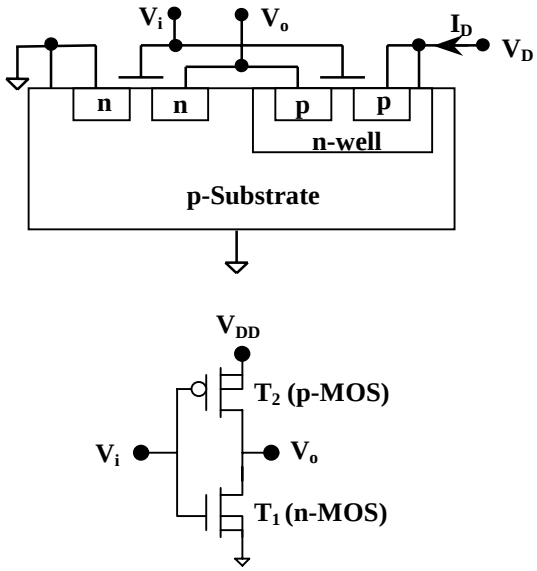


Fig. 6 MOSFET "off" current versus "on" current.

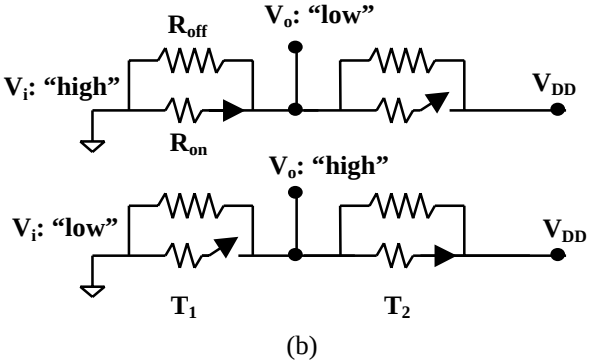
One method for a MOSFET to approach the behavior of an ideal switch is the use of two threshold voltages for one device. When a MOSFET is "on", the threshold voltage is low for maximum "on" current and when it is "off", the threshold voltage is changed to a higher value, reducing the "off" current. This can be done through a voltage applied to the device substrate, known as back or body bias, at the cost of added circuit complexity. It is not used routinely, but is used in some advanced circuits.

Complementary MOSFETs

Complementary MOS circuits consist of n-channel and p-channel MOSFETs connected in series. The basic functional unit of CMOS logic is the binary voltage inverter of Fig. 7(a), shown in cross section and as an equivalent circuit. The device is fabricated by first forming an n-type region or n-well in the p-substrate. Then n-type source and drain are formed in the p-substrate for the n-channel device and p-type source and drain are formed in the n-well for the p-channel device. The two drains are connected, forming the output node V_o and the two gates, tied together, form the input node V_i. For input voltage V_i "high", say 2.5 V, a channel is formed in the n-channel device, turning it on. The same input voltage turns the p-channel device off. Similarly, a zero input voltage turns the p-channel device on and the n-channel device off. Hence, for either "low" or "high" input, one of the devices is "off" and the other is "on". This has important implications for low power circuits, because the current flowing through the "off" device is very low.



(a)



(b)

Fig. 7 (a) CMOS circuit cross section and circuit diagram, (b) simple equivalent circuits for "high" and "low" input voltages.

The "off" device has a very high resistance and the current I_D is near zero for either state. This is the key to CMOS circuits, the standby current, i.e., the current during either one of its two logic states is very low, making for low power dissipation in steady state. The device of Fig. 7(a) can be represented by the simple equivalent circuits of Fig. 7(b). For high V_i, the n-channel transistor T_1 is "on", making it effectively a short circuit and the output voltage V_o is low, i.e., it is near ground potential or zero. It is not exactly zero, because the "on" device has a finite channel or "on" resistance, R_{on}, between source and drain. Similarly, the "off" device allows a small leakage current to flow, because the MOSFET "off" resistance, R_{off}, is not infinite, although it is very high. For low V_i the p-channel transistor is "on" and the output voltage is approximately V_{DD}. The circuit in Fig. 7 is known as an inverter, because "high" input produces "low" output and vice versa.

Power Considerations

The power dissipated by a device is the energy consumed per unit time. The relationship between energy and power is

$$E = \int_0^{t_o} P(t)dt \tag{6}$$

where E is the energy, P the power, and t_0 the operation time. The power dissipated in CMOS circuits is due to three dissipation paths, given by[7]

$$P = P_{switch} + P_{sc} + P_{off} = \alpha f C V_{DD}^2 + I_{sc} V_{DD} + I_{off} V_{DD} \tag{7}$$

where α is the switching activity (the number of times the node makes a power-consuming voltage transition in one clock period), f the frequency, C the capacitance that is charged and discharged during each switching cycle, V_{DD} the supply voltage, I_{sc} the short-circuit path in the short time interval during switching when both n-channel and p-channel are "on" due to finite rise and fall times of the input waveform, and I_{off} the subthreshold leakage current and other leakage currents such as the reverse-biased drain junction leakage current. The "off" current is typically a few nanoamperes leading to a few milliwatts of power dissipation at room temperature, but it increases with increasing temperature. The short circuit power dissipation is usually also relatively low, leaving the switching power as the main power dissipation mechanism.

The energy due to a switching event is given by

$$E = E_{switch} = CV_{DD}^2 \tag{8}$$

Equations (7) and (8) clearly show that reducing the frequency will lower power consumption, but will not change the energy to perform a given operation. Since it is energy consumption that determines the battery life, it is important to reduce the energy rather than just the power. Power, of course, is critical for heat dissipation considerations.

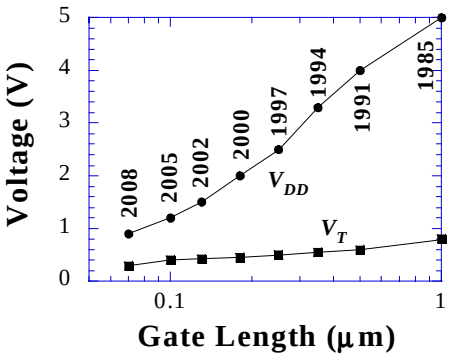


Fig. 8 Supply (V_{DD}) and threshold (V_T) voltages as a function of gate length.

Equation (7) clearly shows that the most effective way to reduce power dissipation is by reducing the supply voltage. This is what has happened over the years, as shown in Fig. 8, where V_{DD} and V_T are shown as a function of gate length and the years when devices with those gate lengths were first put into, or are projected to be put into, production. Power dissipation can also be addressed by varying the frequency of the circuit. For example, when a laptop computer is running on batteries, the circuit may operate at a lower frequency than when it is ac-line powered, where power dissipation is less important.

Figure 8 clearly shows both supply and threshold voltage to have been reduced over the years, but the threshold voltage has not kept pace with this reduction. The main reason for this discrepancy is the rapidly increasing "off" current when V_T is reduced, as discussed above. As Eqn. (2) indicates, when the factor (V_{DD}-V_T) is reduced, as shown in Fig. 8, the "on" current suffers. This, in turn affects the propagation delay time, t_d.

The propagation delay time can be understood by considering the time to charge a capacitor. When a time-varying voltage is applied to a circuit containing a capacitor C, the current flowing in the capacitor is the displacement current I given by

$$I = C\frac{dV}{dt} \tag{9}$$

leading to the propagation delay or charging time

$$t_d = \frac{C\Delta V}{I} \tag{10}$$

where ΔV is the voltage swing which is typically the voltage from zero to V_{DD} or V_{DD} to zero. Using the current expression from Eqn. (2) yields the device propagation delay time

$$t_d = \frac{CV_{DD}}{I_D} = \frac{2LC}{W\mu_{eff}C_{ox}V_{DD}(1-V_T/V_{DD})^2} = \frac{K}{C_{ox}V_{DD}(1-V_T/V_{DD})^2} \tag{11}$$

with $V_G=V_{DD}$. As shown in Fig. 8, the V_T/V_{DD} ratio increases with each device generation leading to increasing delay times. The normalized propagation delay time

$$t_{d,norm} = \frac{t_d}{K} = \frac{1}{C_{ox}V_{DD}(1-V_T/V_{DD})^2} = \frac{t_{ox}}{K_{ox}\varepsilon_o V_{DD}(1-V_T/V_{DD})^2} \tag{12}$$

is plotted in Fig. 9. Here t_{ox} is the oxide thickness, K_{ox} the oxide dielectric constant, and ε_o the permittivity of free space ($8.854\text{x}10^{-14}$ F/cm). This figure shows the very strong dependence of propagation delay time on supply voltage and clearly illustrates the trade-off between power dissipation and delay time. Low supply voltage leads to low power dissipation, but also to longer delay times or slower circuit operation.

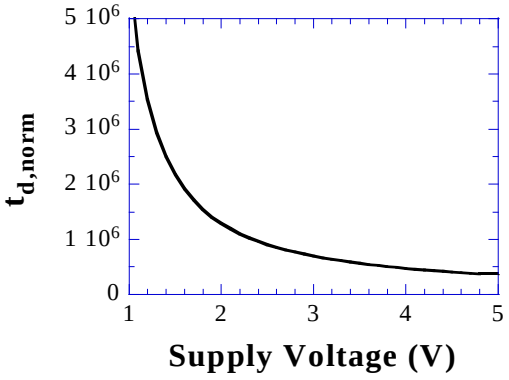


Fig. 9 Normalized propagation delay time versus supply voltage; V_T = 0.5 V, t_{ox} = $5\text{x}10^{-7}$ cm.

Experimental propagation delay data are shown in Fig. 10 versus supply voltage as a function of channel length for bulk Si and silicon-on-insulator (SOI) devices. The important observations in Fig. 10 are that the propagation delay time increases with decreasing supply voltage, that short channel devices are better than longer channel devices, and that SOI performs better than bulk Si. It is very obvious from these two figures that reduced supply voltages have a degrading effect on delay time. Unfortunately, low supply voltages are dictated by both low-power and reliability considerations. As device dimensions shrink, electric fields in the device increase unless the voltages are also reduced. High electric fields lead to reliability problems due to hot or energetic electrons/holes creating damage in the oxide and at the oxide-semiconductor interface. Reduced voltages lead to enhanced reliability but also to lower "on" currents and longer propagation delay times.

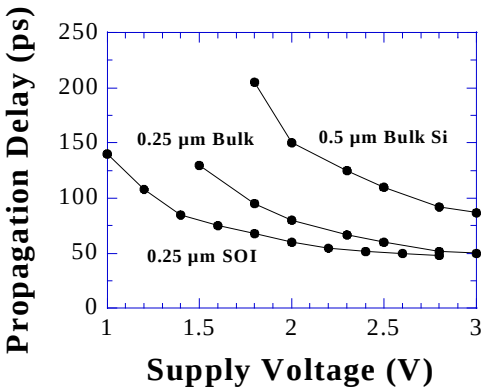


Fig. 10 Propagation delay time versus supply voltage for bulk Si and SOI.

Silicon-on-Insulator

Almost all of today's silicon ICs are fabricated on bulk Si wafers as they have been for the past 40 years or so. While such substrates are well suited for the high complexity of today's circuits, there are other silicon approaches that can be used and have the potential of enhanced performance. Two problems with bulk Si for low-power electronics, are the inability to reduce the threshold voltage sufficiently due to the higher "off" current and to reduce the capacitance. Both of these problems are somewhat alleviated by silicon-on-insulator technology.

SOI wafers differ from bulk Si wafers through the existence of a buried oxide layer (BOX) overlaid by a thin Si layer, as illustrated in Fig. 11. The Si layer is typically 200 – 400 nm thick in the starting wafer and about 100 nm or less after device fabrication. Circuits fabricated on such wafers can operate at lower power and higher fre-

quencies than equivalent circuits fabricated on bulk Si wafers.

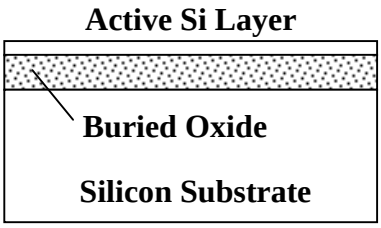


Fig. 11 Silicon-on-insulator wafer.

The two methods for producing SOI wafers are: SIMOX wafers are formed by oxygen implantation into bulk Si wafers followed by appropriate anneals (SIMOX stands for Separation by IMplanted OXygen) and BESOI wafers are formed by bonding two oxidized wafers followed by annealing, lapping and etching (BESOI stands for Bond and Etch Back SOI) or cleaving of hydrogen implanted wafers (Smart Cut).[8] In the SIMOX approach, oxygen is implanted into bulk Si wafers at a dose of around 10^{18} cm^{-2}. The wafers are subsequently annealed at temperatures around 1300°C for several hours to form a high-quality buried oxide and to regenerate the crystalline quality of the active Si layer. The resulting buried oxide is typically 100 – 400 nm thick and the active Si layer on top of the BOX is typically 200 – 400 nm thick.

In the BESOI method, two oxidized Si wafers are brought into intimate contact and they bond by van der Waal's forces. Subsequent annealing increases the mechanical strength of the bond. One of the wafers is then thinned to the desired thickness by mechanical polishing or chemical etching. The oxide, formed by thermal oxidation prior to bonding, can have thicknesses from several hundred to several thousand nm. Similarly, the overlying Si film thickness can vary from 50 nm to 50 μm or more. BESOI wafers require two starting wafers, the handle wafer and the wafer that ultimately ends up as the active layer. Since the active layer is very thin (on the order of a micrometer) and the starting wafer is 600-700 μm thick, most of the second wafer is discarded during the lap/polish/etch process.

A variation of BESOI is the Smart Cut technique in which H^+ is implanted through the oxide of one of the wafers before bonding. The implanted hydrogen forms small cavities at a depth determined by the implantation energy. When the wafer is bonded to the handle wafer and heated to around 500°C, thermal energy causes the hydrogen cavities of the H^+-implanted wafer to merge and the wafer shears due to stress along the implant damage plane, leaving a thin Si layer bonded to the thick handle wafer. The thin bonded layer is then polished and annealed at around 1000°C. Since only about a micrometer of the upper wafer remains bonded to the handle wafer, the remaining wafer can be used as the next handle wafer.

SOI devices have a number of advantages over bulk Si devices. These include: simpler processing, smaller and denser chips, latchup elimination, reduced subthreshold swing allowing lower threshold voltage, lower "off" current and higher "on" current, reduced junction and wiring capacitance, easier to scale to smaller device dimensions, easier device isolation, less crosstalk between digital and analog circuits, good noise margin, increased alpha particle immunity leading to lower soft error rates, and less plasma damage during processing. Latchup is a phenomenon that can occur when a circuit contains pnpn junctions sufficiently close together that when two of the three junctions are forward biased, the system latches, i.e., it switches into its low-impedance state. CMOS circuits on bulk wafers contain pnpn junction combinations and are subject to latchup. Once latchup occurs, the power supply must be turned off resulting in a loss of dynamically stored information. In SOI CMOS circuits, the n-channel and p-channel MOSFETs can be physically isolated thereby eliminating latchup.

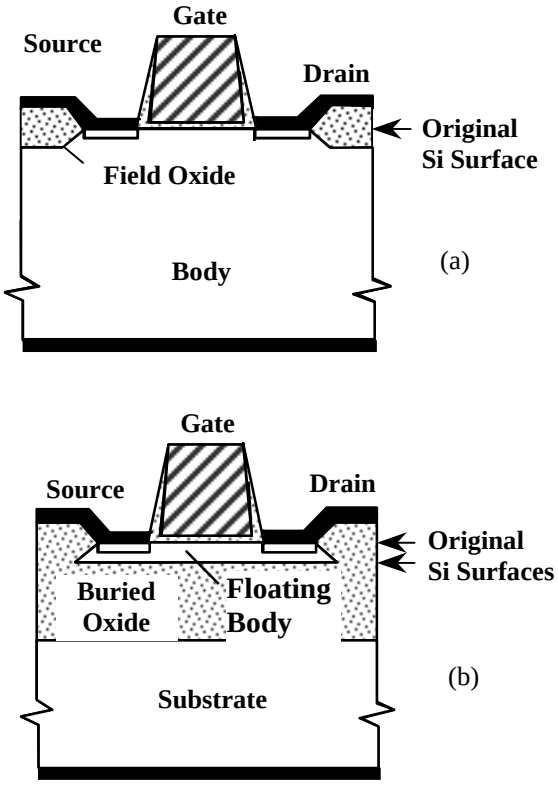


Fig. 12 (a) Bulk MOSFET and (b) SOI MOSFET.

SOI also has disadvantages. These include more expensive wafers, higher defect densities in the active Si layer, floating body effects, and limited computer automated design tools. The floating body comes about for the following reason. When Si is oxidized, a portion of the Si wafer is consumed and turned in SiO_2. The consumed Si is about 45% of the oxide thickness. This is illustrated in the cross section of a bulk Si MOSFET in Fig. 12(a). The regions to the left of the source and to the right of the drain have a thick oxide, known as the field oxide. The oxide has "eaten" its way into the Si wafer. This also happens in SOI wafers, but when the oxide, which grows from the top, reaches the buried oxide, it leaves the non-oxidized Si as a floating Si island or floating body in Fig. 12(b). This island is totally surrounded by oxide because the Si in the surround is completely consumed during the oxidation step. The advantage of this configuration is that adjacent devices are isolated from one another electrically, because they are surrounded by the insulating SiO_2. While an electrically floating body eliminates latchup, it can lead to circuit instabilities, because its voltage is not always well controlled. Nevertheless, the advantages of SOI over bulk Si dominate over the disadvantages and SOI is a serious contender for low-power electronics.

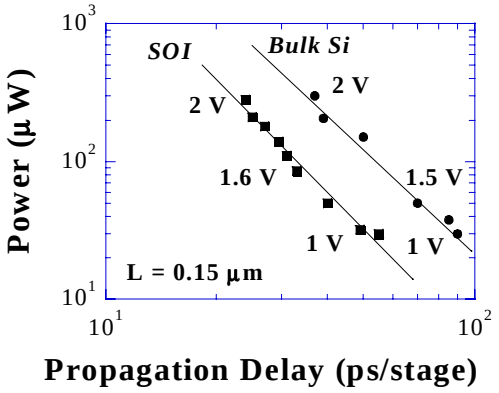


Fig. 13 Experimental inverter delay times and power dissipation for bulk Si and SOI CMOS inverters.[9]

A good demonstration of SOI's low-power ability is shown in Figs. 10 and 13. Fig. 13 shows the power dissipation versus propagation delay per inverter stage for both bulk Si and SOI.[9] For a given delay time, SOI has lower power consumption and for a given power consumption, SOI exhibits lower delay times.

Summary

Low-power electronic circuits are important for portable devices. Semiconductor devices are at the heart of these circuits with MOS devices making up the majority of today's integrated circuits. In digital circuits, the MOSFET can be considered a switch, but it is a non-ideal switch with an "on" resistance and limited current drive in the "on" state and a leakage or "off" current in the "off" state. Both of these non-idealities play a role in circuit behavior. The limited "on" current limits the speed with which a capacitor can be charged and the "off" current leads to power dissipation when the circuit is "off". It is increasingly difficult to limit the power consumption since the trend is to higher frequencies and higher chip densities. Such techniques as dynamic threshold voltages, multiple threshold voltages, and multiple frequencies on one chip help where power dissipation issues are important. Replacing bulk Si with SOI substrates also helps to reduce power consumption. The various limitations of semiconductor devices for low-power applications have been outlined here.

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