CHARGE BURSTS THROUGH DIELECTRIC LAYERS OF 4H-SiC/SiO_2 METAL OXIDE SEMICONDUCTOR CAPACITORS

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ABSTRACT

Small bursts of inversion layer charge in 4H-SiC metal oxide semiconductor capacitors leak through the oxide layer leading to discontinuities during capacitance-time measurements. These, in turn lead to difficulties in generation lifetime extraction. This behavior has been observed using non-equilibrium capacitance-time (*C-t*) and current-time (*I-t*) measurements, at room temperature and at 400 °C.

INTRODUCTION

Silicon carbide is a unique compound semiconductor because, in addition to being ideally suited for high temperatures, extreme environments, and high power devices, it has the same native oxide as silicon – silicon dioxide. Consequently, intense research has been pursued toward developing a commercially viable SiC MOSFET, as it would offer better performance than its silicon counterpart in many situations. Although problems still exist, it is reasonable to predict that a SiC MOSFET will become commercially available in the near future. For this reason, reliability of SiC MOSFETs is an important concern [1].

Many of SiC's useful properties are due to its wide band gap. Paradoxically, the wide band gap also causes a major reliability concern for the dielectric, since it gives substantially smaller oxide-semiconductor energy barriers than those of the standard Si/SiO_2 system. Thus, dielectric breakdown is worse for SiC/SiO_2, both by time-zero [2] and time-dependent dielectric breakdown (TDDB) [3] measurements. In addition, F-N tunneling current is higher than in silicon [4], and is worse at high temperatures [5]. Furthermore, it has been found that SiC/SiO_2 devices suffer from negative bias temperature instability (NBTI), which is also a major reliability issue for silicon devices [6]. Reliability troubles at elevated temperatures are especially concerning, as SiC is desirable for its high temperature properties.

In the following work, we present evidence which suggests that sudden bursts of inversion charge flow through the dielectric layer of 4H-SiC/SiO_2 MOS capacitors (MOS-C) in deep-depletion, without causing destructive breakdown. Evidence consistent with this theory is presented in the time-dependent capacitance (*C-t*) and current (*I-t*) behavior, at room temperature and at 400 °C.

Phenomena involving the nondestructive breakdown of silicon MOS capacitors have been studied for many years [7-9]. The transient current observed by Jackson et al. during TDDB measurements includes current spikes in a silicon MOS-C which are fundamentally similar to the behavior we are reporting [9]. However, to the best of the authors' knowledge, this behavior has not been previously reported in either SiC/SiO_2 or Si/SiO_2 MOS capacitors during the transition from deep-depletion to inversion.

EXPERIMENTAL

MOS capacitors (MOS-C) were formed from n-type 4H-SiC samples, grown with Dow Corning chlorosilane/propane chemistry. The 20 µm epitaxial layers were nitrogen doped to an approximate concentration of 10^{16} cm^{-3}. A 45 nm SiO_2 layer was grown thermally, and passivated with NO. Molybdenum gate contacts with gold overlayers (each ~150 nm) were sputtered in Ar and circular contacts of approximate diameters of 377 and 675 µm were patterned using photolithography. The devices were measured in an electrically isolated probe station with a maximum temperature of 400 °C.

The fundamental purpose of our work is to characterize carrier generation lifetime (τ_g) of 4H-SiC epitaxial layers using the pulsed MOS-C technique, originally suggested by Zerbst [10], and detailed in [11]. The basic procedure starts with an MOS capacitor in accumulation (V_G = 5 V); and the gate voltage is switched to an inversion bias level (V_G = -10 V). The inversion layer does not form immediately, since minority carriers must be thermally generated. Thus, as the inversion layer forms, the space charge region (scr) width below the gate decreases and the capacitance increases. The speed and behavior of this recovery contain information about the generation lifetime in the scr of the device. The MOS-C recovery time depends on the generation rate, which is proportional to the intrinsic concentration, n_i. At room temperature, n_i in 4H-SiC is about 500 cm^{-3} and the generation rate is negligible. Thus we use the probe station's maximum temperature of 400 °C, which brings n_i to about 10^8 cm^{-3}, and reduces the pulsed MOS-C recovery time to several minutes.

RESULTS AND DISCUSSION

It was observed that some of our SiC MOS capacitors have a discontinuity in the *C-t* curve as indicated by points (a) and (b) in Fig. 1. The proposed explanation for this behavior is the following: during the recovery from deep depletion, inversion charge slowly builds up at the oxide-semiconductor interface. The electric field across the oxide continually increases, due to the increasing inversion and gate charge. Eventually, most of the gate voltage is dropped across the oxide and the oxide field becomes very high, as illustrated in the band diagram of Fig 2 (a). For example, the oxide electric field of the device pulsed to V_G = -10 V is about 2 MV/cm in strong inversion. At points (a) and (b) in Fig. 1, a momentary charge flow occurs, which results in some of the inversion charge drifting through the dielectric. This is indicated by the sudden lowering of the capacitance, which is directly proportional to the charge in the inversion layer. Since the gate voltage is constant, this loss of inversion charge redistributes the potential within the MOS-C such that the highest electric field is now located in the substrate and not in the oxide, as illustrated by Fig. 2 (b). This is why the breakdown is not destructive: the instant the inversion charge begins flowing through the oxide, the electric field in the oxide lowers. Furthermore, since only limited amount of inversion charge exists, only a small amount of charge can move through the oxide until additional inversion charge is generated – a process which takes a relatively long time. Thus, the event has a built-in negative feedback which protects the device, in a similar manner to a circuit breaker. If the

device were in accumulation, breakdown would be more likely to occur.

The charge which escapes through the oxide is proportional to the size of the capacitance drop – thus it is higher for point (b) on Fig. 1 than point (a), because the electric field is higher at point (b) than at point (a). To quantify this charge loss, we use the equation derived in ref. [12]:

$$\Delta Q = \frac{V_0 C_{ox}^3}{2}\left(\frac{1}{C_f^2} - \frac{1}{C_i^2}\right) \quad (1)$$

where $V_0 = -qK_s\varepsilon_0 N_D/C_{ox}^2$, C_{ox} is the oxide capacitance, C_i is the capacitance before the loss and C_f is the final capacitance. For example, using the parameters for the device in Fig. 1 and values of 16 pF and 13.2 pF for C_i and C_f, respectively, we find that 7.4×10^{-8} C/cm^2 is lost during charge burst labeled (b). In addition, the exact electric field at which the burst occurs can also be calculated. If the charge burst occurs when the device is inversion, the surface potential is approximately twice the bulk Fermi potential ($2\phi_F$) and the electric field is given by the expression $(V_G - V_{fb} - 2\phi_F)/t_{ox}$ where V_G is the gate bias during the measurement, V_{fb} is the flatband voltage and t_{ox} is the oxide thickness. However, if the burst occurs during the transient, the equation relating electric field to capacitance in a non-equilibrium MOS-C must be used [12]:

$$\mathcal{E}_{ox}(t) = \frac{V_G - V_{fb}}{t_{ox}} + \frac{qN_D K_s \varepsilon_0}{2t_{ox}}\left(\frac{1}{C(t)} - \frac{1}{C_{ox}}\right)^2 \quad (2)$$

where $C(t)$ represents the capacitance at the time of the burst.

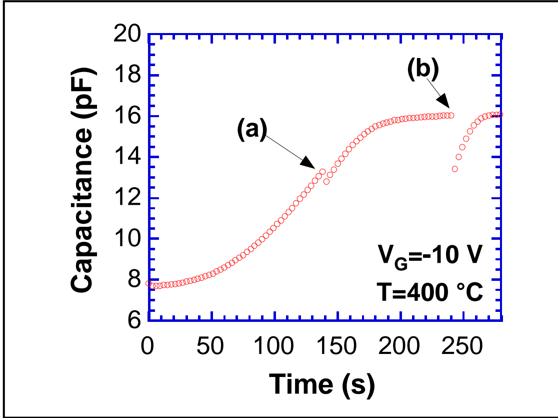

FIGURE 1. CAPACITANCE VERSUS TIME WITH DISCONTINUITIES THAT INDICATE BURSTS OF CHARGE THROUGH THE GATE OXIDE.

In order to further characterize this behavior, a measurement was made which employed the same bias sequence as above, but current, instead of capacitance, was monitored as a function of time. The device behavior was the same as in the previous experiment: electron-hole generation causes the inversion layer to form and the scr width decreases. However, current, unlike capacitance, is inversely proportional to the width of the scr. Thus, the measured current is continually decreasing until a full inversion layer is formed. At this point, the current flow ceases because the device is in equilibrium. Of course, when the oxide permits the flow of leakage current (as is often the case in SiC-MOS capacitors) the final current will be constant, with a magnitude equal to the lesser of the true oxide leakage current or the generation current. This procedure, combined with the above method form the basis of a generation lifetime measurement technique, first suggested by Calzolari [13].

During this process, sometimes a discontinuity occurs in the *I-t* curve (Fig. 3) which is consistent with that observed in the *C-t* behavior of Fig. 1. Again, when the inversion charge is lost, the scr width increases to a value held at some previous time. In Fig. 3, this scr widening manifests itself as a higher current, caused by the larger volume of carrier generation.

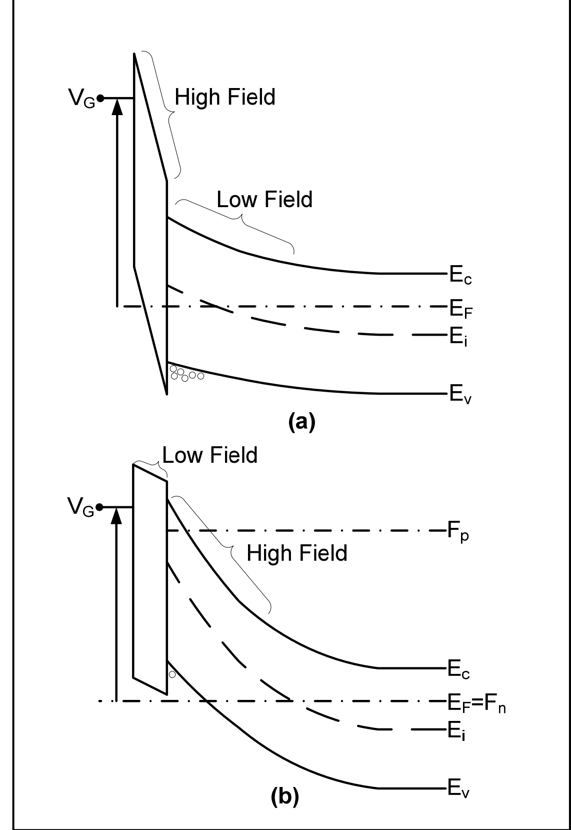

FIGURE 2. BAND DIAGRAM OF AN N-TYPE MOS-C (A) IMMEDIATELY BEFORE AND (B) AFTER THE CHARGE BURST INDICATING THE RELAXATION OF THE OXIDE ELECTRIC FIELD.

It is again possible to quantify the magnitude of the charge lost. Perhaps the simplest approach to this is to find the capacitances corresponding to initial and final currents where the break occurred. The equation relating current to capacitance in a deep-depletion MOS-C (neglecting surface generation) is [13]

$$\frac{I(t)}{1 - C(t)/C_{ox}} = \frac{-qK_s\varepsilon_0 A_G^2 n_i}{\tau_{g,eff}}\left(\frac{1}{C(t)} - \frac{1}{C_{inv}}\right) \quad (3)$$

where $I(t)$ is the current measured at time t, $\tau_{g,eff}$ is the effective minority carrier generation lifetime, and C_{inv} is the capacitance when a full inversion layer is present. Provided the doping concentration is sufficiently low that there is negligible displacement current during the return to equilibrium, the left hand side of (3) reduces to $I(t)$ and the capacitance can be written in terms of the measured current as

$$C(t) = \left(\frac{1}{C_{inv}} - \frac{I(t)\tau_{g,eff}}{qK_s\varepsilon_0 A_G^2 n_i}\right)^{-1} \quad (4)$$

Using (4) one finds the capacitances corresponding to the currents immediately before and after the break and uses (1) to quantify the charge loss.

A final experiment uses the fact that the room temperature generation rate is negligible in 4H-SiC, due to the extremely low intrinsic carrier concentration. Thus, if we use a light source to introduce generation to form an inversion layer, once the source is removed and the device settles to equilibrium it should ideally have a constant capacitance. However, if inversion charge is lost through the oxide, the capacitance will decrease to reflect the resulting increase in scr width. This procedure was originally described by Sheppard et al. [14] to as a simple method of checking for oxide leakage in SiC-MOS capacitors and experimental data were later presented by Cheong et al. [15]. A sample plot is given in Fig. 3, which has discontinuities that indicate, as seen previously, that charge has escaped through the oxide. This case is especially interesting because it shows that the behavior is present even at room temperature. In fact, this method is a convenient way to check the oxide quality on a SiC-MOS capacitor since it does not require high temperatures. The analysis of the charge loss is the same as with the high temperature C-t measurement; the lost charge is given by (1).

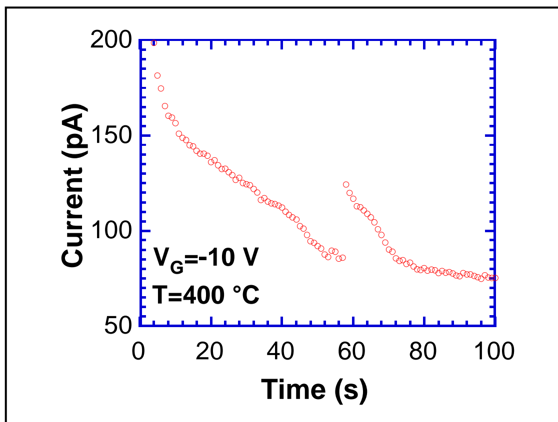

FIGURE 3. CURRENT VERSUS TIME WITH DISCONTINUITIES THAT INDICATE BURSTS OF CHARGE THROUGH THE GATE OXIDE.

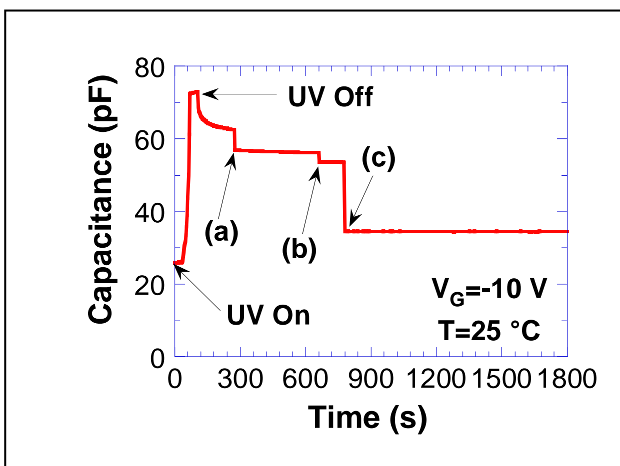

FIGURE 4. CAPACITANCE VERSUS TIME AT ROOM TEMPERATURE. DISCONTINUITIES INDICATE A BURST OF CHARGE THROUGH THE GATE OXIDE.

A similar phenomenon in silicon devices has been investigated by Klein et al. [7]. The mechanism for single-hole self healing dielectric breakdown in Si/SiO_2 MOS capacitors was thought to be the thermalization of a weak point in the dielectric caused by a high electric field. It is also reasonable to assume that this dielectric thermalization is due to a high local electric that forms around a flaw at the interface, rather than a weak spot in the oxide. The proposed mechanism is the following: as the inversion layer forms, the electric field in the oxide increases. Thus, at a weak point in the oxide or a flaw at the interface which causes a high local electric field, the soft dielectric breakdown described above is initiated. As mentioned earlier, as soon as part of the inversion layer begins to flow to the gate, the electric field across the oxide quickly relaxes. Thus, the breakdown is not allowed to continue long enough for the damage to become destructive. This hypothesis is supported by the fact that charge bursts can be nearly eliminated by lowering the oxide electric field through a combination of lower gate voltage and thicker oxide.

Although a specific flaw which is known to cause a high local electric field at the SiC/SiO_2 interface is not known at this time, there are several possibilities. It is well known that SiC materials generally have significant dislocation densities compared to traditional materials. Closed core screw dislocations and threading edge dislocations are two common defects which are parallel to the [0001] direction (c-axis). Since SiC is generally sliced at an angle tilted slightly away from the c-axis, these defects may intersect the Si/SiO_2 interface as indicated in Fig. 5. It is reasonable to consider, based on the space charge theory of dislocations [16], that a high field may surround the points at which defects intersect the surface.

As second possibility is that the high field is due to a flaw created during the thermal oxidation of SiC. It has been observed that some carbon remains at the interface after thermal oxidation [17-19]. This rough, carbon rich transition region between SiC could result in a point on the interface where a high local electric field forms, or cause a weak spot in the oxide.

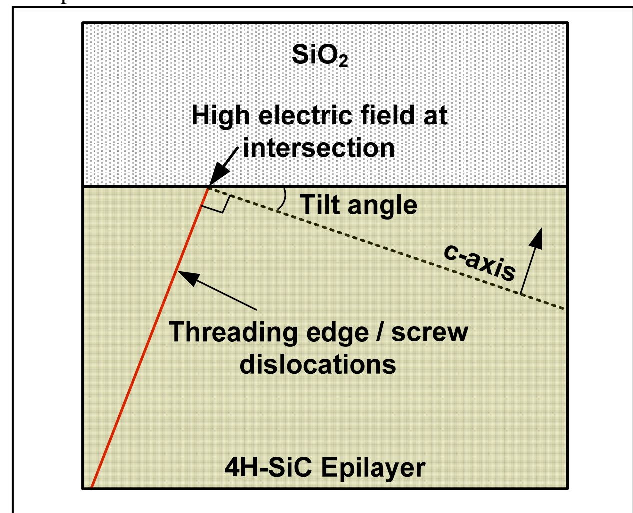

FIGURE 5. 4H-SIC MOS CAPACITOR WITH DEFECTS INTERSECTING THE SIC/SIO_2 INTERFACE AND CREATE A HIGH LOCAL ELECTRIC FIELD.

This phenomenon could potentially impact the reliability of SiC MOSFETs. In a MOSFET, this behavior might manifest itself as a sudden, temporary decrease in drain current, although the entire event would be extremely fast since the lost inversion layer carriers would instantly be restored by the source. In fact, the abundant availability of carriers removes the negative feedback safety mechanism described above. More specifically, once the charge flow initiates, carriers from the source will almost instantly replace the ones lost, and thus the electric field across the oxide will not relax. Therefore, if this type of event occurs in a SiC MOSFET, it seems

reasonable to conclude that destructive breakdown of the gate dielectric would occur.

In addition, the SiC MOS-C has been considered as a candidate for a non-volatile floating memory [15], as well as for use as a charge coupled device (CCD) [20]. In a non-volatile memory element, the effect of a charge burst would be to change the state of the device, since the presence of an inversion layer generally indicates whether the device is in the “1” or “0” memory state. In a CCD, charge bursts would add excess charge, resulting in an erroneous signal.

CONCLUSION

A soft-breakdown phenomenon has been experimentally observed in a unique way, in which discontinuities appear in the time dependent capacitance and current behavior of 4H-SiC/SiO_2 MOS capacitors. The proposed explanation is that a fraction of inversion charge bursts through the oxide layer of a 4H-SiC/SiO_2 MOS-C. To the best of the authors’ knowledge, this behavior has not been previously studied in this manner in silicon or SiC MOS capacitors, although similar behavior has been observed in silicon devices using different methods. This phenomenon could affect the reliability of future SiC MOS devices.

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