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CORONA-OXIDE-SEMICONDUCTOR DEVICE CHARACTERIZATION

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Abstract—We describe a novel contactless semiconductor characterization technique capable of determining a number of semiconductor material and device parameters. It consists of charge deposited on a semiconductor sample from a corona source and the subsequent measurement of surface voltage as a function of time using a Kelvin probe. Both positive and negative charge can be deposited to create a variety of surface conditions. For oxidized samples, the technique yields oxide thickness, net oxide charge, mobile oxide charge and effective oxide charge density, interface trap density, and flatband voltage. For junction devices it yields the near surface doping density, and generation lifetime. When coupled with optical excitation, the technique can be further extended to determine the minority carrier lifetime. © 1998 Published by Elsevier Science Ltd. All rights reserved

1. INTRODUCTION

Many semiconductor material and device parameters are determined with relatively simple test structures. Among these, MOS capacitors (MOS-Cs) and p–n junction or Schottky diodes lend themselves to a surprisingly large number of parameter determination. For example, oxide thickness, fixed and mobile oxide charge, oxide trapped charge density, interface trap density, doping density, recombination and generation lifetime, band offsets, and work function difference can be determined with MOS-Cs. Traditionally these measurements have been made by depositing a permanent gate (metal or poly-Si) or using a temporary mercury gate on an oxidized wafer. A different approach is discussed in this article. The physical gate is replaced with a deposited charge from a corona source giving a corona charge-oxide-semiconductor (COS) device. This has the decided advantage of being rapid and contactless, thereby adding to the repertoire of contactless characterization techniques.

A most attractive feature of COS characterization is the contactless nature of the measurement. A variety of semiconductor material and device parameters can be determined with his technique. These include generation lifetime of COS capacitors pulsed into deep depletion, flatband voltage, oxide thickness, various oxide charge densities, interface trap density, and doping density. When coupled with optical excitation, the technique can be further extended to determine the minority carrier lifetime.

We discuss in this article the physics and application of the corona-oxide-semiconductor technique to semiconductor material and device characterization and illustrate the technique with a few examples. To see how this technique contrasts with conventional MOS measurements, we made a series of measurements on specially prepared wafers, combining COS and MOS measurements to determine the generation lifetime.

2. CORONA-OXIDE-SEMICONDUCTOR CHARACTERIZATION

The corona charge technique is a method for semiconductor characterization developed by IBM, East Fishkill, during 1983–1992[1–4]. However, until recently there was no commercial instrumentation and the technique was only used sparingly. Recently, it was developed into a commercial product[5]. We give an introduction to this technique here, review the relevant theory and compare the technique to the well established MOS technique. Then we illustrate the technique with generation lifetime measurements of COS devices.

The technique is illustrated in Fig. 1. Positive or negative charge from a corona source is deposited on the semiconductor sample surface. The corona source ionizes room air using a high voltage source. The corona ionic species are predominantly CO_3^- and H_3O^+ for negative and positive ions, respectively. The corona source forces a uniform flow of ionized air molecules toward the wafer surface. The

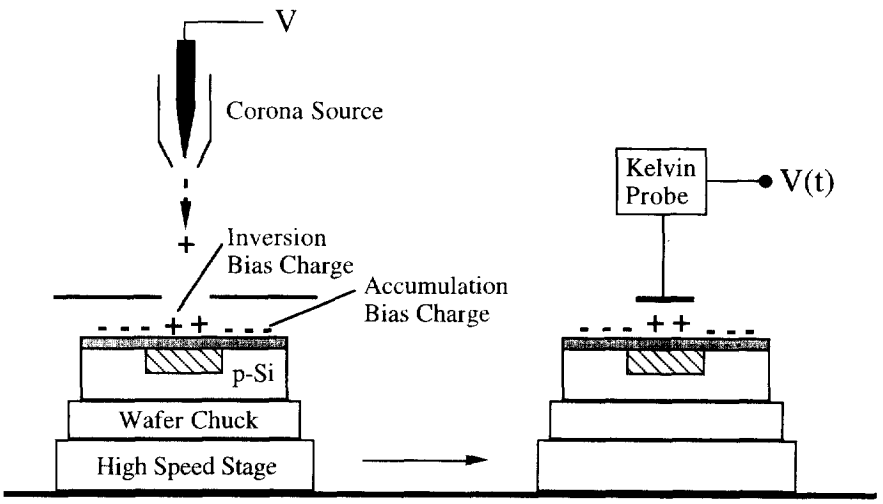

Fig. 1. Corona-pulsed deep-depletion measurement apparatus.

very short (approximately 0.1 μm) atmospheric mean free path of ionized gas ensures that the molecules retain very little kinetic energy during the process. The large area (~5 mm diameter) charge is determined by a well defined aperture. In the example of Fig. 1, negative charge is deposited locally on an oxidized *p*-Si wafer to bias the substrate into accumulation. Next positive charge is deposited in one of two modes illustrated in Fig. 2. The ability to deposit both negative and positive charge has the distinct advantage over MOS-C measurements of providing a guard ring with a near zero gap between guard ring and active area, reducing perimeter generation. The corona bias system consists of a needle connected to a high-voltage source, coupled with hardware that forces a uniform flow of ionized air molecules toward the wafer surface.

In the first mode (Fig. 2(a)), the positive charge pulse, deposited in the center of the negatively charged area with $+Q_G > |-Q_G|$, drives the device from accumulation into deep depletion, where Q_G is the charge density deposited on the sample. In the second mode, the positive charge pulse also drives the device from accumulation into deep depletion. The device is then allowed to reach inversion (Fig. 2(b)). Subsequently, a second positive charge pulse drives the device from inversion into deep depletion. In this mode, with the surface inverted during the transient measurement, interface electron–hole pair (ehp) generation is reduced significantly and only the substrate bulk properties are measured.

Once the charge pulse is deposited, we have to determine the transient response of the device. In conventional MOS devices, the capacitance is measured as a function of time. For COS measurements, the sample moves on a high speed stage from the corona source to a Kelvin probe (see Fig. 1) where the voltage is measured as a function of time as thermal ehp generation causes the reverse-biased space-charge region to collapse with a concomitant voltage decrease.

2.1 *Generation lifetime*

The COS generation lifetime is similar to the pulsed MOS-C generation lifetime measured by driving an MOS-C from accumulation or from inversion into deep depletion. The MOS-C is well understood and a number of techniques were proposed to analyze the capacitance–time data[6–8]. A common method is to pulse the MOS-C into deep depletion, keep the gate voltage constant and measure the capacitance transient as shown in Fig. 3(a). With $V = Q/C$ = constant, both the charge Q and the capacitance C change as a function of time. The gate charge increases as some of the thermally generated holes, indicated by the open circles in the shaded space-charge region, flow around the circuit to be deposited on the gate.

The gate voltage is ramped in a related technique, illustrated in Fig. 3(b), with the capacitance remaining constant with time[9]. In the pulsed COS technique, the charge remains constant. With $Q = CV$ = constant, both V and C vary, as shown in Fig. 3(c). Figure 3 shows all three approaches; (a) voltage is constant, (b) capacitance is constant, (c) charge is constant. We now derive the appropriate equations for lifetime extraction.

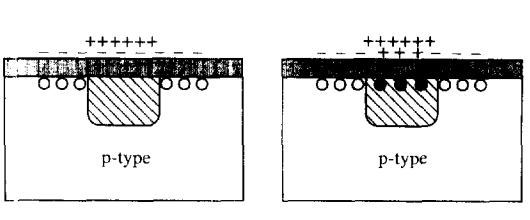

Fig. 2. Semiconductor substrate pulsed into deep-depletion from (a) accumulation, (b) inversion.

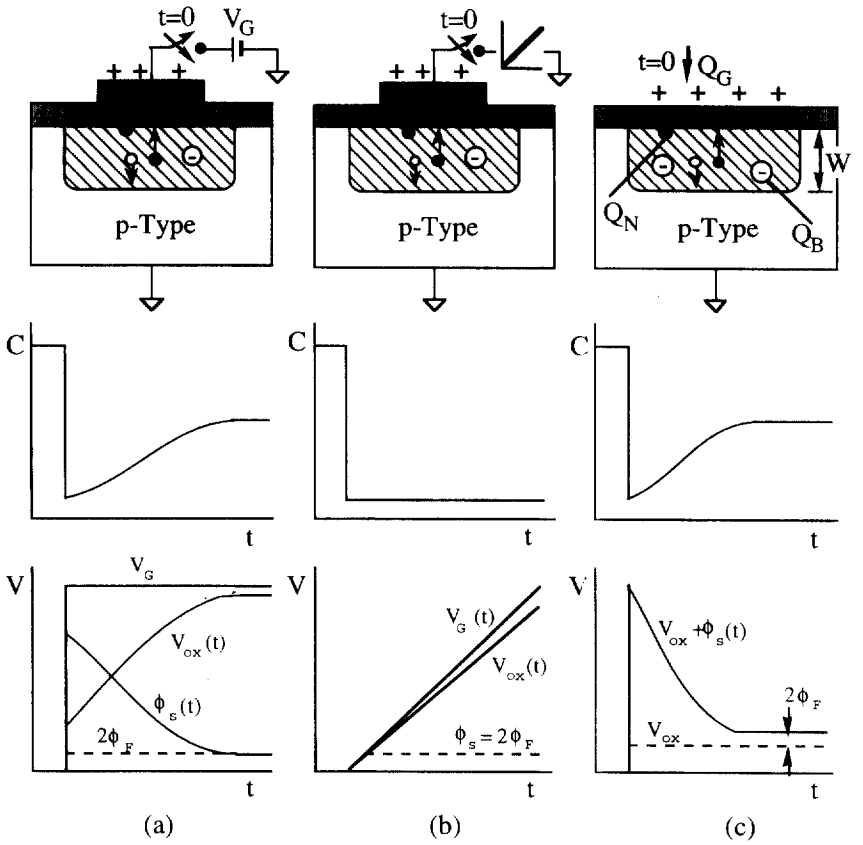

Fig. 3. Schematic and time dependence of the capacitance, gate voltage, oxide voltage, and surface potential for (a) pulsed MOS-C, (b) ramped MOS-C, (c) pulsed COS-C.

The gate voltage of an MOS-C or COS-C is given by;

$$V_G = V_{FB} + V_{ox} + \phi_s \tag{1}$$

where V_{FB} is the flatband voltage, V_{ox} the oxide voltage, and ϕ_s the surface potential. V_G is the gate voltage for an MOS-C or the surface voltage for an COS-C and V_{ox} is given by;

$$V_{ox} = Q_G/C_{ox} = -Q_S/C_{ox} \tag{2}$$

where Q_G is the gate charge density and Q_S the semiconductor charge density. We use the term "surface voltage" because for the COS approach there is no gate, understanding, of course, that gate voltage in MOS and surface voltage in COS are identical. Equation (1) becomes;

$$V^*_G = \phi_s - Q_S/C_{ox} = \phi_s + (Q_N + Q_B)/C_{ox} \tag{3}$$

where $V^*_G = V_G - V_{FB}$, Q_N is the inversion charge density, and Q_B the bulk charge density.

2.1.1. *COS-C-Constant charge.* After corona charge is deposited on the gate, Q_G remains constant throughout the measurement, causing V_{OX} to remain constant too. This constancy has been verified by mapping measurements. Differentiating Equation (1) leads to;

$$\frac{dV_G}{dt} = \frac{d\phi_s}{dt} \tag{4}$$

assuming the flatband voltage to be invariant with time, *i.e.*, $dV_{FB}/dt = 0$. This is a good approximation for room temperature measurements.

The bulk charge density is;

$$Q_B = qN_A W = \sqrt{2qK_S\epsilon_0 N_A \phi_s} \tag{5}$$

where W is the space-charge region width. With Q_G and Q_S constant with time, we get;

$$\frac{dQ_S}{dt} = 0 = -\frac{dQ_N}{dt} - \frac{dQ_B}{dt} = -\frac{dQ_N}{dt} - qN_A\frac{dW}{dt} \tag{6}$$

or using Equation (5)

$$-\frac{dQ_N}{dt} = \sqrt{\frac{qK_S\epsilon_0 N_A}{2\phi_s}}\frac{d\phi_s}{dt} = \frac{K_S\epsilon_0}{W}\frac{d\phi_s}{dt} = \frac{K_S\epsilon_0}{W}\frac{dV_G}{dt} \tag{7}$$

2.1.2. *MOS-C-Constant voltage.* For the pulsed MOS-C with constant gate voltage after the device is driven into deep depletion, the capacitance is measured as a function of time. In that case, dQ_N/dt is given by[8];

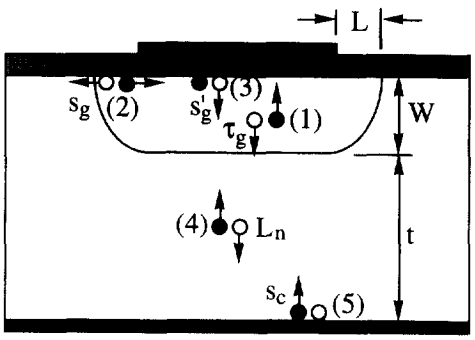

Fig. 4. Five thermal generation mechanisms of a reverse-biased MOS-C.

$$-\frac{dQ_N}{dt}=\frac{qK_s\epsilon_o N_A C_{ox}}{C^3}\frac{dC}{dt} \tag{8}$$

2.1.3. *MOS-C-Constant capacitance.* For the ramped MOS-C with constant capacitance after the device is driven into deep depletion, the capacitance is measured for various ramp rates. In that case, dQ_N/dt is given by[9];

$$-\frac{dQ_N}{dt}=\frac{C_{ox}dV_G}{dt} \tag{9}$$

For COS measurements, the surface voltage is monitored as a function of time; for MOS measurements, it is either the capacitance that is measured as a function of time or the constant or saturation capacitance for various ramp rates.

To be able to extract material/device parameters, we need to know dQ_N/dt. It is the rate at which inversion carriers are generated in the non-equilibrium, deep-depleted semiconductor. There are five sources of thermal carrier generation illustrated in Fig. 4, assuming optical and impact ionization carrier generation to be absent, i.e., the measurement is made with the sample in the dark at voltages below semiconductor breakdown. Generation rates are ehp generation (1) in the space-charge region (scr), (2) at the surface in the lateral portion of the scr, (3) at the surface under the gate, (4) in the quasi-neutral bulk, and (5) at the back surface. The generation rates of the five mechanisms can be written as[6];

$$G_{(1)}=\frac{qn_i(W-W_{min})}{\tau_g};\quad G_{(2)}=\frac{qn_i s_g A_L}{A_G} \tag{10a}$$

and

$$G_{(3)}=qn_i s_g;\ G_{(4+5)}=\frac{qn_i^2 D_n}{N_A L'_n} \tag{10b}$$

where τ_g is the generation lifetime, s_g the surface generation velocity of a depleted surface, and s'_g the surface generation velocity of an inverted surface. Generation rates (4) and (5) are coupled into an effective minority carrier diffusion length L'_n, given by:

$$L'_n=L_n\frac{\cosh(\zeta)+(s_c L_n/D_n)\sinh(\zeta)}{(s_c L_n/D_n)\cosh(\zeta)+\sinh(\zeta)} \tag{11}$$

with $\zeta = t/L_n$, L'_n is the minority carrier diffusion length, D_n the minority carrier diffusion coefficient, and s_c the surface generation velocity at the back surface. The reason for choosing the effective generation width to be $W - W_{min}$ where W_{min} is the final or minimum scr width when the device is in inversion equilibrium, was discussed thoroughly[6,8].

The lateral extent of the scr is generally not known. Assuming the lateral extent to be identical to the vertical extent gives $A_L = 2\pi r(W - W_{min})$ and $A_G = \pi r^2$, where r is the gate radius for a circular gate. The generation rates in Equation (10a) are W-dependent, whereas those in Equation (10b) are not. We rewrite Equation (10) as;

$$G=\frac{qn_i(W-W_{min})}{\tau_{geff}}+qn_i s_{geff} \tag{12}$$

where,

$$\tau_{geff}=\frac{\tau_g}{1+2s_g\tau_g/r};\ s_{geff}=s'_g+\frac{n_i D_n}{N_A L'_n} \tag{13}$$

The generation rate in Equation (12) is the negative of the rate of change of the inversion charge density (minority electrons are negatively charged), i.e.,

$$\frac{dQ_N}{dt}=-\sum G \tag{14}$$

giving;

$$\frac{dQ_N}{dt}=\frac{qn_i(W-W_{min})}{\tau_{geff}}+qn_i s_{geff} \tag{15}$$

Equations (7)–(9) now become;

$$\frac{dV_G}{dt}=\frac{qn_i W}{K_s\epsilon_o}\left(\frac{(W-W_{min}}{\tau_{geff}}+s_{geff}\right) \tag{16}$$

$$\frac{1}{C^3}\frac{dC}{dt}=\frac{n_i}{K_s\epsilon_o N_A C_{ox}}\left(\frac{(W-W_{min})}{\tau_{geff}}+s_{geff}\right) \tag{17}$$

and

$$\frac{dV_G}{dt}=\frac{qn_i}{C_{ox}}\left(\frac{(W-W_{min})}{\tau_{geff}}+s_{geff}\right) \tag{18}$$

One of the advantages of the COS approach is the constancy of the charge. With Q_G constant, V_{ox} also remains constant in contrast to conventional MOS-C measurements, where V_{ox} increases as a function of time, as shown in Fig. 3. This increasing oxide voltage during the capacitance decay limits the voltage that can be applied to a gate because of oxide breakdown or oxide current limitations. Oxide breakdown, of course, is terminal. However, even if the oxide is not driven into breakdown, problems can still arise.

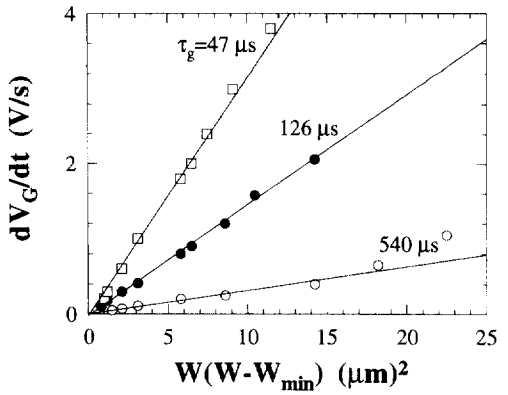

Fig. 5. COS generation lifetime plot.

It is possible for V_{ox} to become sufficiently high for appreciable oxide or gate current to flow. Gate current for a p-type substrate consists of electrons injected from the substrate into the oxide and then to the gate. These electrons come from the thermally generated inversion layer. Since some of these electrons are injected into the oxide, it will take longer to build up the inversion layer. In other words, it will appear as if the generation lifetime is longer than it actually is[10]. No such problem exists in the COS method because the oxide voltage remains constant during the measurement. One simply chooses an oxide voltage for which gate current is negligible.

Equations (16) and (18) give the time dependence of the gate voltage on the generation rate and Equation (17) gives the time dependence of the capacitance. Equation (17) is the basis of the well known Zerbst method[11]. To demonstrate the validity of the COS generation lifetime model, we measured three oxide-Si samples by varying the pulse charge magnitudes to obtain various space-charge region widths. The dependence of the voltage rate of change on $W(W - W_{min})$ is shown in Fig. 5. The linear relationship is in good agreement with the prediction of Equation (16). The slopes of these lines give τ_{geff}. All lines intersect at the origin, implying s_{geff} to be negligible. This demonstrates that the COS charge induced junction is very effective in limiting interface generation.

To compare MOS and COS measurements, we fabricated and measured a number of wafers. Silicon wafers, 200 mm in diameter, n-type, (100)-orientation of 10 Ω cm resistivity were prepared as shown in Fig. 6. Some wafers were ion implanted. The generation lifetime, flatband voltage, oxide thickness, and doping density were measured by the corona charging method. Aluminum contacts were then evaporated and the generation lifetime and doping density of these wafers were remeasured using the constant voltage pulsed MOS-C technique. Care was taken to make the MOS measurements on devices at those locations of the wafer close to the original COS measurements, which, of

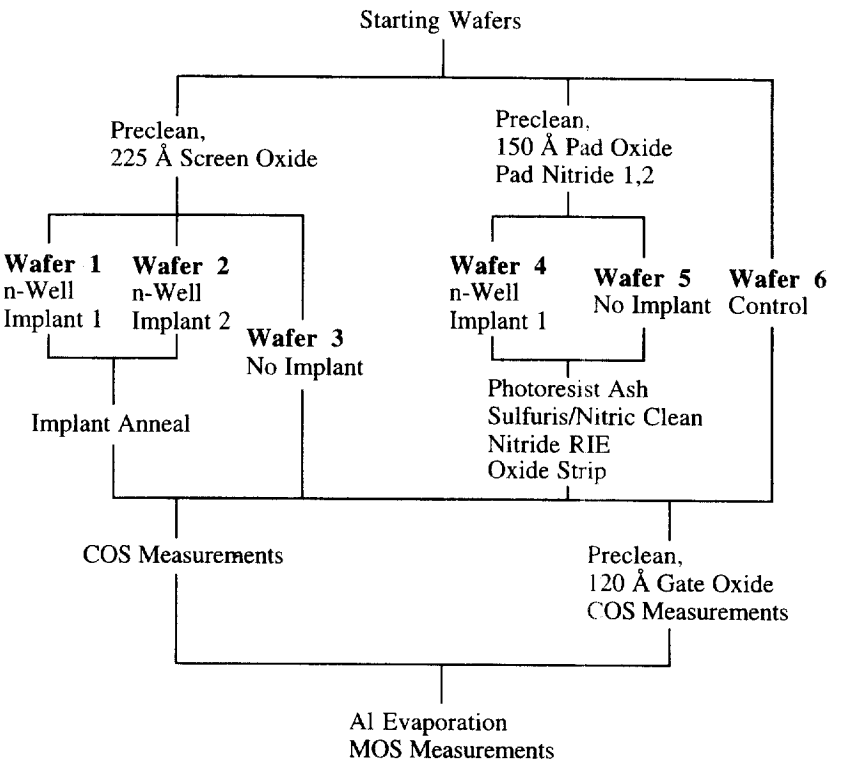

Fig. 6. Wafer preparation process flow.

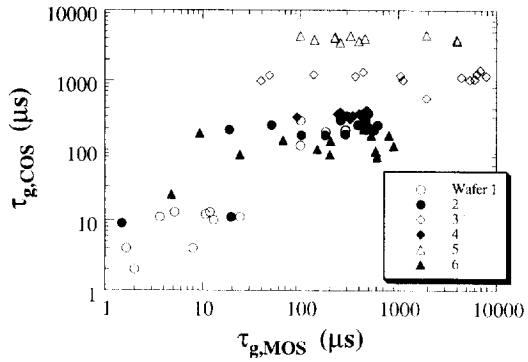

Fig. 7. Effective generation lifetimes determined by the COS and MOS techniques.

course, were made without gates. Wafers without implantation were used for control.

The MOS and COS effective generation lifetimes are shown on Fig. 7. There is general agreement between the two methods, though there is some local variation. The doping densities in these wafers varied from $2\times10^{14}\,\mathrm{cm}^{-3}$ to $3\times10^{16}\,\mathrm{cm}^{-3}$. The agreement between the two methods is better in the lower τ_g range. For the higher lifetimes, the COS values are tightly bunched, whereas the MOS values show significant scatter. Two reasons for this are proposed. MOS lifetime measurements are inherently influenced by lateral surface generation, which is difficult to suppress. Surface generation has a larger influence as the generation lifetime increases. Such surface generation is better controlled in COS measurements because the charge induced guard ring is located next to the device, with virtually no gap.

The second reason can be found in the rather defective oxides of these samples (not shown in this article). During MOS measurements, the oxide voltage increases with time, causing part of the inversion layer to drain into the gate through weak spots in the oxide. This extends the transient capacitance time response, causing artificially high generation lifetimes. One of the advantages of COS measurements is the insensitivity of the measurement to localized oxide defects. Such localized defects merely discharge the deposited corona charge locally, since charge beyond the defect cannot flow into the defective area because of poor lateral oxide conduction. This is in contrast to MOS measurements, where the conductive gate channels charge from the entire gate area into defective areas, even if these are microscopic areas.

Although the emphasis of this article is on generation lifetime, we will briefly include surface doping density and flatband voltage measurements. The COS implementation of flatband voltage measurement in COS has a unique advantage over MOS measurements.

2.2. *Near surface doping density*

Near surface doping density is a measure of the average doping density in the top few microns of the semiconductor. This near surface doping density is determined in the COS technique by forming a field-induced junction and pulsing it into deep depletion, similar to pulsed MOS measurements. The data analysis is similar to that of MOS measurements. The junction is formed by first creating an accumulation region at the test site. Then, an inverted region is created in the center of this test site. The accumulation region acts as a guard ring, suppressing lateral conduction to give the junction a well defined area.

The junction is then pulsed into deep depletion with an additional charge ΔQ and the resulting voltage transient is recorded. The deposited charge is imaged in the substrate by repelling majority carriers to a space-charge region width W_{dd}. As minority carriers are generated, the scr collapses in time and returns to its equilibrium width W_{inv} and equilibrium voltage V_{Si}. During the measurement, the charge increment ΔQ and the transient voltage increase ΔV_{Si} are measured. Doping density is a function of these two variables, $N_D = f(\Delta Q, \Delta V_{Si})$.

The determination of the doping density follows from the following equations. W_{dd} and ΔQ are given by:

$$W_{dd} = W_{min} + \Delta W \tag{19}$$

$$\Delta Q = qN_D\Delta W \tag{20}$$

The voltage during the depleting pulse is;

$$\Delta V_{Si} + V_{Si} = \frac{qN_A W_{dd}^2}{2K_s\epsilon_o} \tag{21}$$

where V_{Si} and space-charge region width W_{inv} are related by;

$$V_{Si} = \frac{qN_A W_{min}^2}{2K_s\epsilon_o} \tag{22}$$

V_{Si} is also given by[12];

$$V_{Si} = \frac{kT}{q}\left[2.1\ln\left(\frac{N_A}{n_i}\right) + 2.08\right] \tag{23}$$

Equations (19)–(23) are solved iteratively for N_A.

A comparison between N_A measured by COS and MOS-C for *n*-epitaxial layers is shown in Fig. 8. For the MOS-C, the C_{max}–C_{min} method was used to determine N_A[6]. In this method, the ratio of the minimum to maximum capacitance yields N_A.

2.3. *Flatband voltage*

One of the parameters that must be known for proper interpretation of COS data is the flatband voltage V_{FB}. For MOS capacitors, the flatband voltage is the gate voltage corresponding to the flatband capacitance C_{FB}. C_{FB} can be calculated if the oxide thickness and substrate doping density are

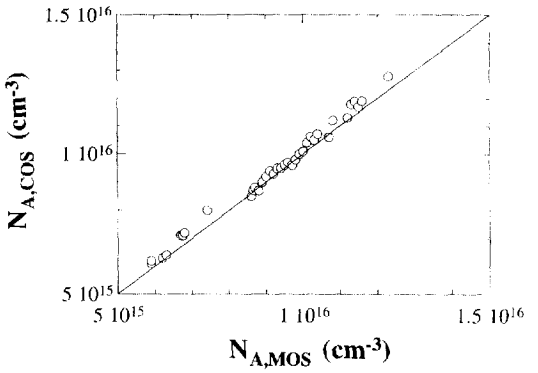

Fig. 8. Doping density determined by COS and MOS techniques. The line represents perfect correlation between the two.

known. In COS measurements, the flatband voltage is determined by measuring the voltage with and without illumination[4].

The theory of MOS capacitors is well known. The semiconductor charge density Q_S for a p-type semiconductor in depletion or inversion is:

$$Q_S = -\sqrt{2kTK_S\epsilon_0 n_i}F(U_S, \Lambda) \tag{24}$$

where the F function is defined as[13]:

minating the device. With constant corona charge, equivalent to constant semiconductor charge or constant F, according to Equation (24) the locus of the $F - U_S$ plot is along a horizontal line such as the dashed line. It is obvious from Fig. 9 that the surface potential decreases with increasing excess carriers created by illuminating the device. In the limit of high illumination, $U_S \to 0$, i.e., $\phi_S \to 0$.

From Equations (1) and (2) we find:

$$V_{G,dark} = V_{FB} + Q_G/C_{ox} + \phi_S \tag{26}$$

Without illumination, the voltage is given by Equation (26). With intense illumination, $\phi_S \to 0$ and

$$V_{G,light} \approx V_{FB} Q_G/C_{ox} \tag{27}$$

For a given corona charge density Q_G, the charge deposited on the oxide remains constant during the measurement, regardless of illumination. Hence, the surface photovoltage $V_{SPV} = V_G(\text{dark}) - V_G(\text{light})$ is:

$$V_{SPV} \approx \phi_S \tag{28}$$

Flatband voltage corresponds to $\phi_S = 0$, i.e., $V_{SPV} \approx 0$, as illustrated in the plot of surface photovoltage vs gate voltage measured under intense illumination in Fig. 10. Flatband voltage is indicated as the point where $V_{SPV} = 0$. Note that determination of V_{FB} in this way does not require a knowledge of oxide thickness or substrate doping density, in contrast to MOS-C flatband voltage determination, where both must be known.

$$F(U_S, \Lambda) = \sqrt{\Lambda(e^{-U_S} + U_S - 1) + \Lambda^{-1}(e^{U_S} - U_S - 1) + \Lambda(e^{U_S} + e^{-U_S} - 2)\Delta} \tag{25}$$

In this expression $\Lambda = p_o/n_i$ (p_o = majority carrier density), U_S is the normalized surface potential $U_S = \phi_S/(kT/q)$, ϕ_S is the surface potential, and Δ is the normalized excess carrier density, defined by $\Delta = \Delta p/p_o$, where $\Delta p = \Delta n$ is the excess carrier density. In the absence of excess carriers, i.e., in equilibrium, the last term in Equation (25) becomes zero.

F is plotted vs U_S in Fig. 9 as a function of the normalized excess carrier density, produced by illu-

3. CONCLUSIONS

We described a novel semiconductor characterization technique in which traditional metal or poly-Si gates are replaced by corona charge. Similarities to conventional MOS techniques are reviewed here.

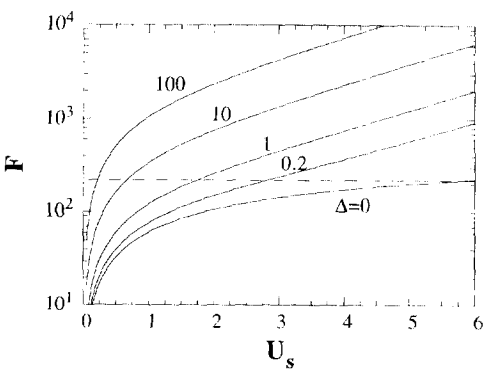

Fig. 9. F function versus normalized surface potential as a function of normalized injection level.

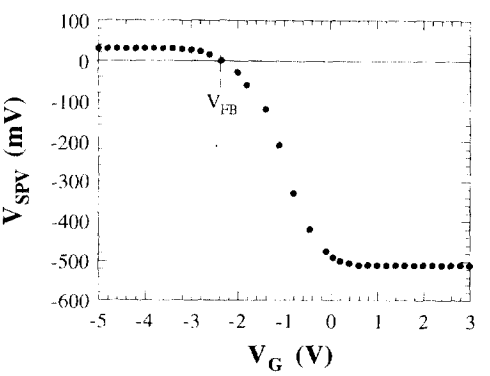

Fig. 10. Surface photovoltage versus gate voltage. $N_A = 2.6 \times 10^{14}$ cm^{-3}.

We show that charge deposition, followed by Kelvin surface voltage sensing, leads to various oxide charge densities, flatband voltage, and oxide thickness determination. By forming junctions, the generation lifetime and surface doping density can be determined. Although not shown here, the technique, when appropriately modified, also gives the minority carrier lifetime. The application of COS generation lifetime measurement is demonstrated on *n*- and *p*-type Si wafers. The equipment is available commercially and adds an important tool to the semiconductor characterization family.

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