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Measurement of carrier generation lifetime in SOI devices

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Abstract

This paper presents a new, simple method of measuring the generation lifetime in SOI (silicon-on-insulator) MOSFETS. Lifetime is extracted from the transient characteristics of MOSFET subthreshold current. Using this technique, generation lifetime was mapped across finished SIMOX (separation by implantated oxygen) wafers, BESOI (bonded and etchedback SOI) wafers, and UNIBOND wafers. BESOI material evaluated in this study had about seven times longer effective generation lifetime than SIMOX material and the three types of the SOI wafers are shown to have a lifetime variation of ±20% across four inch wafers. The generation lifetime was also found to depend on the device fabrication process.

1. Introduction

SOI technology is becoming a promising candidate for future VLSI, as the quality of SOI material continues to improve. Carrier lifetime in SOI films is often used as a process-control measure because of its strong dependence on densities of crystal defects and heavy metal atoms. Carrier lifetime is also known to affect the performance of bipolar and CMOS devices. Several authors have reported generation lifetime measurement methods using SOI MOSFETs [1–6]. However, most of the techniques require complicated data analysis. The purpose of this paper is to propose a simple generation lifetime characterization method without numerical analysis.

2. Analysis

A negative step voltage was applied to the gate of a partially depleted SOI MOSFET (Fig. 1). The front gate voltage was stepped from 1.8 (above threshold) to 0.4 V (subthreshold) with 0.1 V at the drain. Transient drain currents of MOSFETs are observed due to the floating-body nature of the device (Fig. 2) [7–10]. The drain current is suppressed immediately after the negative voltage step and it gradually increases to the steady state value with time. Since the negative voltage step makes the floating body potential negative during the transient, the body effect forces the 'apparent' threshold voltage to increase, resulting in suppressed drain current. The drain current reaches the steady state value as the body potential relaxes back to zero as carriers are generated. The transient time T_0, which is defined as the time for the drain current to reach 90% of its steady-state value, is about seven times larger for the device on BESOI wafers than on SIMOX wafers.

During this transient, carriers are generated to replenish the space–charge region between the steady-state width of $x_{d\infty}$ and the maximum space–charge region width of $x_{d\,max}$. These carriers can be supplied by four sources as shown in Fig. 1. Among the four mechanisms shown in Fig. 1, the bulk generation in the space–charge region described as the mechanism 1 is focused in the following discussion. The time rate of

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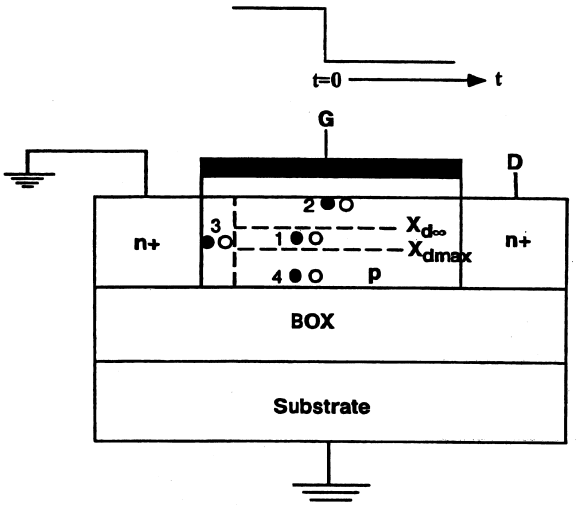

Fig. 1. An SOI MOSFET in pulsed condition. The solid and open circles represent the electron-hole pains being generated. Four distinctive generation mechanisms are shown [11]. The generation mechanism 1, 2, 3 and 4 represent bulk generation in the space–charge region, front surface generation, generation in the source/drain-to-body space–charge region, and backside generation, respectively. $x_{d\,max}$ and $x_{d\,\infty}$ represent the maximum space–charge region width and steady-state space–charge region width, respectively.

change of the space–charge region width x_d is given by Eq. (1) [11, 12]:

$$-qN_a\frac{dx_d}{dt} = q\frac{n_o}{\tau}\left[x_d(t) - x_{d\,\infty}\right] + qn_i s, \tag{1}$$

where N_a is the doping concentration, n_i is the intrinsic carrier concentration, τ is the effective generation lifetime, and s is the effective surface generation velocity.

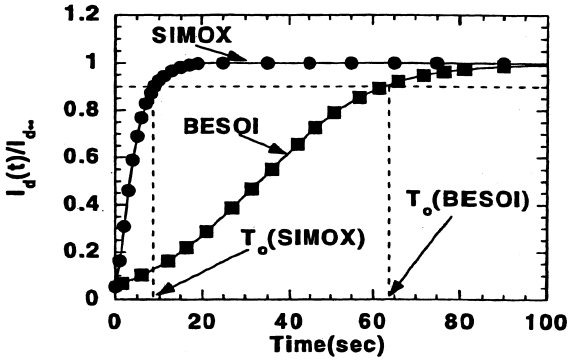

Fig. 2. Typical transient drain current characteristics for floating-body MOSFETs made on a SIMOX wafer and BESOI wafer. The drain current was normalized to the steady-state value of $I_{d\,\infty}$. T_0 (SIMOX) and T_0 (BESOI) represent the transient times of the MOSFETs on SIMOX wafer and BESOI wafer, respectively.

If we assume that the bulk generation in the space–charge region described by mechanism 1 in Fig. 1 is dominant (it will be discussed later), Eq. (1) has the following solution:

$$x_d = \left(x_{d\,max} - x_{d\,\infty}\right)\exp\left(-\frac{n_i}{N_a}\frac{t}{\tau_g}\right) + x_{d\,\infty}. \tag{2}$$

The subthreshold current is proportional to

$$\exp\left\{\frac{q[V_g - V_t(t)]}{\xi(t)kT}\right\},$$

where $V_t(t)$ is the time-dependent 'apparent' threshold voltage, $\xi = 1 + [C_D(t)/C_{ox}]$ and $C_D(t)$ and C_{ox} are the space–charge region capacitance and gate oxide capacitance, respectively [13]. During the transient, the change in $\xi(t)$ is calculated to be less than 5%, which is much smaller than the change in $V_g - V_t(t)$ (which is about 150%) and, therefore, $\xi(t)$ was assumed to be a constant in the following analysis. The transient drain current normalized to the steady state current $I_{d\,\infty}$ is represented by

$$\frac{I_d(t)}{I_{d\,\infty}} = \frac{\exp\left\{\dfrac{q[V_g - V_t(t)]}{\xi kT}\right\}}{\exp\left\{\dfrac{q[V_g - V_{t\,\infty}]}{\xi kT}\right\}} = \exp\left\{\frac{q\gamma\left[\sqrt{2\Phi_f} - \sqrt{2\Phi_f - V_{BS}(t)}\right]}{\xi kT}\right\}, \tag{3}$$

where

$$V_{BS}(t) = -\frac{qN_a}{2\varepsilon_s}\left\{[x_d(t)]^2 - x_{d\,\infty}^2\right\},$$

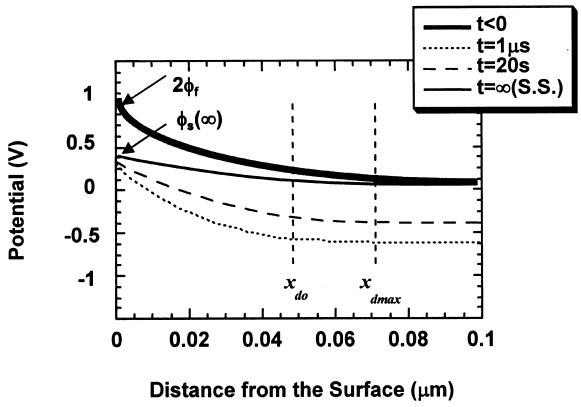

Fig. 3. MEDICI-simulated potential distribution across the silicon film for different times during turn-off. $x = 0$ represents the front surface interface. The body potential abruptly changes by $-2\Phi_f + \Phi(\infty)$ at $t = 0+$ $\Phi(\infty)$ is the surface potential at steady-state. As carriers are generated, the body potential change relaxes back to 0.

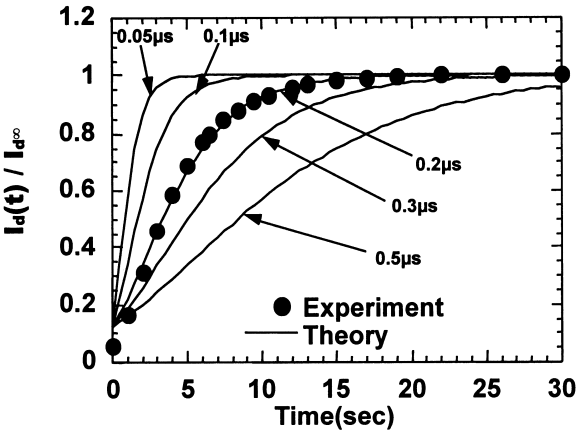

Fig. 4. Calculated transient drain current curves for various generation lifetimes. The measurement data for a SIMOX wafer are also shown. The measurement data match very well with the theoretical curve with 0.2 μs lifetime.

γ is the body effect coefficient. During the transient, the surface potential is not pinned and changes with time as shown in Fig. 3. However, the amount of the change is small and is neglected in Eq. (3). The error from this assumption also decreases as the off-state gate voltage increases. Fig. 4 shows the calculated drain current for different lifetimes. The measured current agrees well with the theoretical curve with 0.2 μs lifetime.

From Eqs. (3) and (2), the relationship of τ_g to the transient time T_0 can be calculated:

$$\tau_g = \frac{\frac{n_i}{N_a} T_0}{\ln\left[\frac{x_{d\,max} - x_{d\,\infty}}{\sqrt{x_{d\infty}^2 + \frac{2\varepsilon_s}{qN_a}\left\{\left[\sqrt{2\Phi_f} + 0.1\frac{\xi}{\gamma}\frac{kT}{q}\right]^2 - 2\Phi_f\right\}} - x_{d\,\infty}}\right]}. \tag{4}$$

For our device with 105 Å gate oxide and 2.2×10^{17} cm^{-3} body doping, Eq. (4) becomes

$$\tau_g = \frac{T_0}{45}, \tag{5}$$

where the units of τ_g and T_0 are in μs and s, respectively. The technique described above should be used for partially depleted devices only. Even for partially depleted devices, when the non-depleted region is as thin as the Debye length, the charge-coupling effect with the buried oxide layer should be taken into account. Since the silicon film thickness of our devices is 1000 Å and the $x_{d\,max}$ is calculated to be about 700 Å, the non-depleted region is about 300 Å thick and Eq. (5) can be used for our devices.

3. Results and discussion

Eq. (5) was used to characterize carrier generation in MOSFETs fabricated on different types of SOI substrates. Fig. 5 shows the distribution of measured generation lifetime across three different types of SOI wafers: SIMOX wafer, BESOI wafer, and UNIBOND wafer. A tight distribution of lifetimes across the wafer was observed. The lifetime in BESOI wafer was longer than that in SIMOX wafer and UNIBOND wafer due to the absence of implantation damage during SOI fabrication. Since the three wafers were processed identically as part of a split lot, the difference in the lifetime comes from the quality difference of the initial SOI substrates.

The generation lifetime also depends on the fabrication process of the devices. Fig. 6(c) shows that the devices with the threshold adjust implant performed through the sacrificial oxide (Early-V_t process in Fig. 6(a)) have longer lifetime than those with the threshold implant performed through the completed gate (Late-V_t process in Fig. 6(b)) for both SIMOX wafer and BESOI wafer [14]. The reason for the difference in the lifetime is probably because the devices with Late-V_t process have less number of subsequent processing steps and therefore the annealing of the implantation-induced damage is less than in the devices with Early-V_t process.

We checked the validity of the earlier assumption that mechanism 1 is dominant. The surface generation velocity (mechanism 2 in Fig. 1) was independently measured on gated-diode structures (Fig. 7). The extracted surface generation velocity was about 3 cm s^{-1} for both SIMOX and BESOI wafers. Therefore, the contribution from the surface generation in the lifetime extraction is very small and is negligible for SIMOX wafer (Fig. 5(a)). The surface contribution is

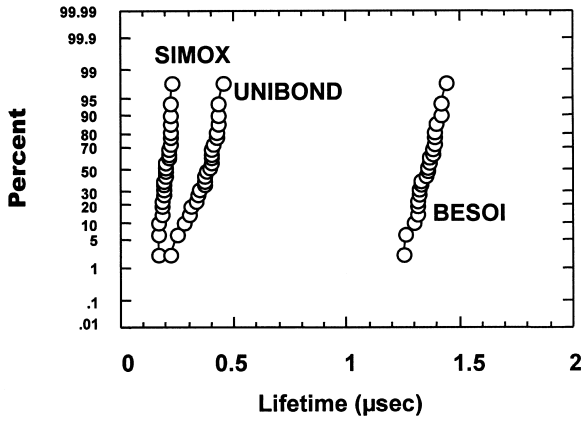

Fig. 5. Generation lifetime distribution obtained by our technique on finished wafers.

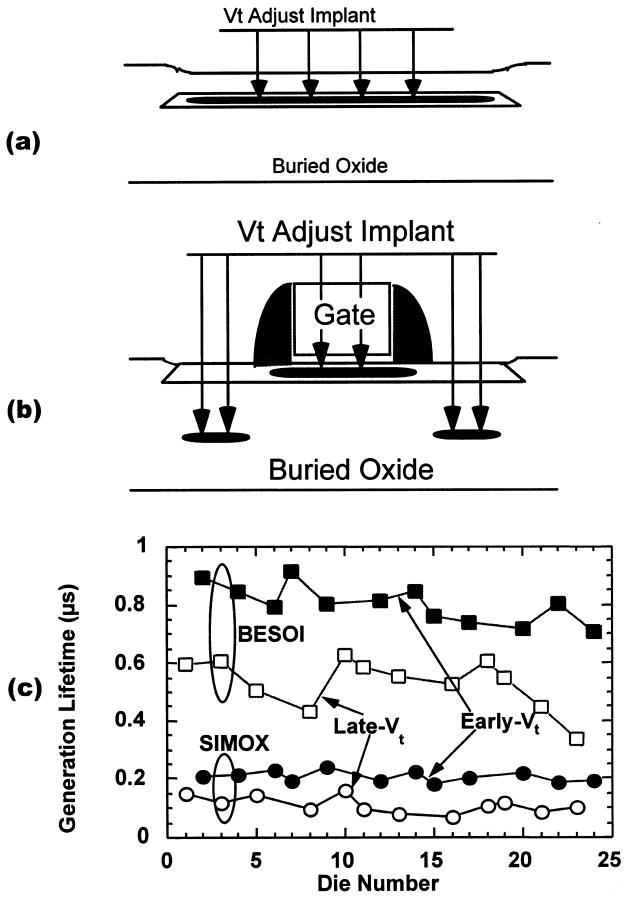

Fig. 6. Comparison of generation lifetime between devices with Early-V_t process (a) and Late-V_t process (b). All the devices are fabricated in the same wafer with checker board pattern for different threshold adjust implantation processes. (c) The generation lifetime in the devices with Early-V_t process is about 60% longer than those with Late-V_t process.

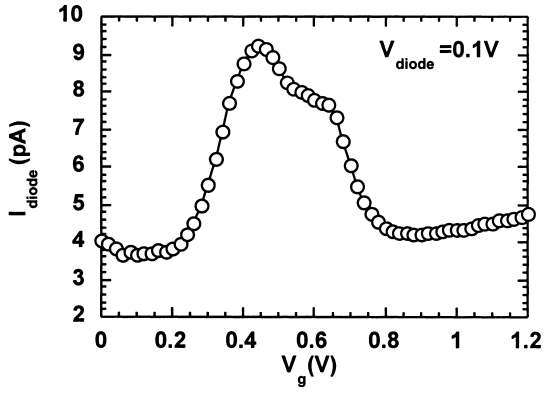

Fig. 7. Current–voltage characteristics of a gate-controlled diode. The surface generation current is about 5 pA from which the surface generation lifetime s of 3 cm s^{-1} was extracted.

no longer negligible for material with longer lifetime such as the BESOI wafer (Fig. 5(b)) and in this case the extracted lifetime should be interpreted as effective lifetime determined from both the bulk and the surface components. A large device with $W/L = 1000/2$ μm was used in the lifetime measurement to minimize the contribution from the generation in device isolation edge and in the source/drain-to-body junction (mechanism 3 in Fig. 1). Fig. 8(a) shows the transient current for different temperatures. Fig. 8(b) shows the transient time T_0 as a function of temperature. The slope of the line in Fig. 8(b) corresponds to the activation energy of 0.57 eV, which is close to the value of half the energy gap in silicon, indicating that the generation inside the space–charge region dominates over the generation from the neutral bulk region and from the back interface (mechanism 4 in Fig. 1) at temperature below 70°C.

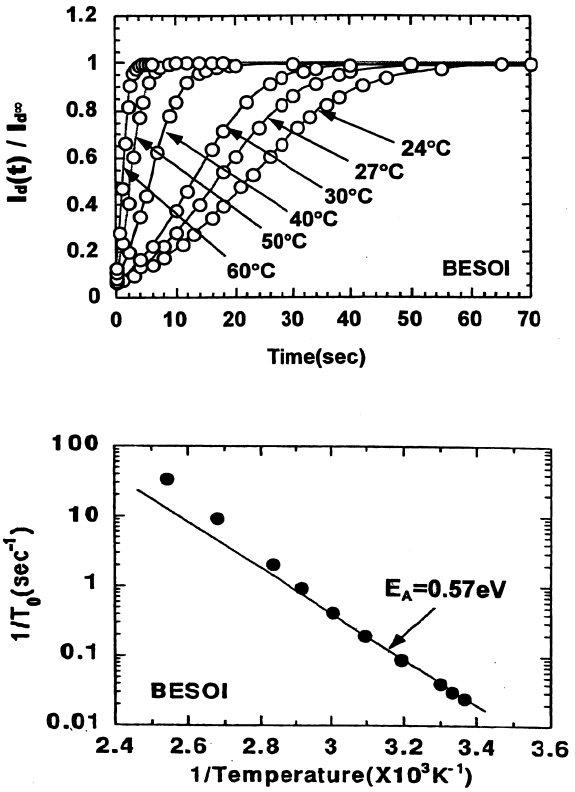

Fig. 8. (a) The transient drain current characteristics for different temperature. (b) The transient time T_0 as a function of temperature. The activation energy E_A of 0.57 eV is obtained from the slope of the line, indicating that the back-side generation is negligible below 70°C.

In order to verify this lifetime measurement method, the lifetime was also measured with another technique previously published [1]. Fig. 9 shows the current transient and numerical analysis results. The lifetime extracted from the slope of the line in Fig. 9 was 0.18 μs, which is very close to the lifetime value of 0.20 μs obtained by our method. Since the front surface was inverted when we performed the technique of Ref. [1], the surface generation component was suppressed. The fact that the extracted lifetimes from the two techniques are almost the same even though the surface is depleted, during measurement with our technique, further confirms that the surface contribution is very small.

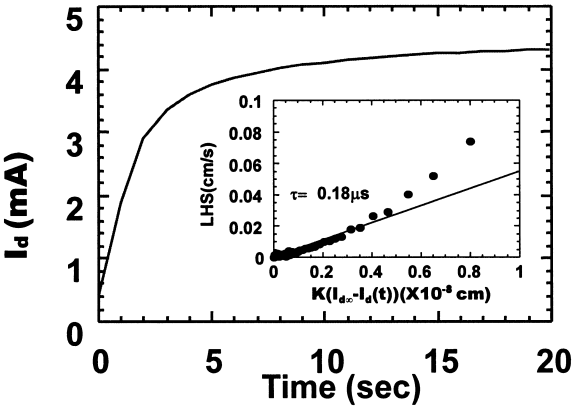

Fig. 9. Current transient and (inset) numerical analysis obtained by the method described by Ioannou et al. [1].

4. Conclusions

In this paper, a new and simple technique for measuring generation lifetime in MOSFETs fabricated on SOI is presented. Transient subthreshold current is measured, from which carrier generation life time can be determined easily without any numerical analysis. Its usefulness has been experimentally demonstrated and proven to provide very sensitive results as a function of different SOI materials and fabrication processes. Lifetime mapping on different types of SOI wafers shows a lifetime variation of ±20% across a four inch wafer.

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