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Thin p/p$^+$ epitaxial layer characterization with the pulsed MOS capacitor

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Abstract

The defect properties of thin p/p$^+$ wafer are not as easily characterized as those of bulk wafers. Recombination lifetime and minority carrier diffusion length measurements do not work well for thin layers, but generation lifetime characterization is eminently suitable. However, for thin epitaxial layers it is difficult to determine the correct generation lifetime because the linear portion of the Zerbst plot is too small to extract the generation lifetime when the applied gate voltage confines the space-charge region (scr) to the lightly doped epitaxial layer. For low gate voltages, moreover, the Zerbst slope is higher then that at high gate voltages. A sufficiently high gate voltage extends the scr to the out-diffused p$^+$ region. However, if the scr reaches the p$^+$ region, there is a drop off in the Zerbst plot. We have developed a mathematical analysis for this region. We have also extended the analysis to the measurement of possible p/p$^+$ interface imperfections, e.g. misfit dislocations. © 1998 Elsevier Science Ltd. All rights reserved.

1. Introduction

As device size shrinks, defect densities and metallic contamination in semiconductors become more important because they increase leakage currents and degrade gate oxide integrity (GOI). Epitaxial (epi) and denuded wafers are often used because these layers contain fewer defects, fewer metallic contaminants and lower oxygen densities than bulk wafers. Moreover, heavily doped p$^+$ substrates prevent latch-up triggering, are good absorption buffers of alpha particles and the p$^+$ substrates are effective getters. To prevent latch-up in small CMOS devices, the epi thickness should decrease as CMOS devices shrink [1] because the effective parasitic carrier path length determines the parasitic *npn* or *pnp* emitter to base resistance and current gain. Hence, the demand on epi wafers increases continuously and the importance of thin layer characterization increases as device size shrinks.

It is more difficult to characterize the electrical properties of epitaxial layers than bulk wafers because the epi layers are generally very thin compared to the minority carrier diffusion length. Recombination lifetime (τ_r), measurement methods, such as surface photovoltage (SPV) and photoconductance decay (PCD) are very convenient and popular to evaluate bulk wafers because they are relatively simple, contactless and require less time than pulsed MOS capacitor measurements [2]. However, the measurements are difficult to interpret for layers thinner than the diffusion length. Photoluminescence (PL) can be used, provided the optically generated excess carriers are confined to the epitaxial layer [3]. Other methods, such as the optical precipitate profiler (OPP) [4] and double crystal X-ray diffraction with mapping capability (DCDM), are also used to evaluate thin layers [5]. However, OPP has poor depth resolution and it just counts the number of physical defects. DCDM is a qualitative method and sometimes it is difficult to obtain rocking curve separation in thin epi wafers. Hence, generation lifetime measurements are one of few characterization methods to evaluate thin layers, quantitatively.

A common method to determine generation lifetimes (τ_g) is the Zerbst technique [2]. An ideal Zerbst plot is

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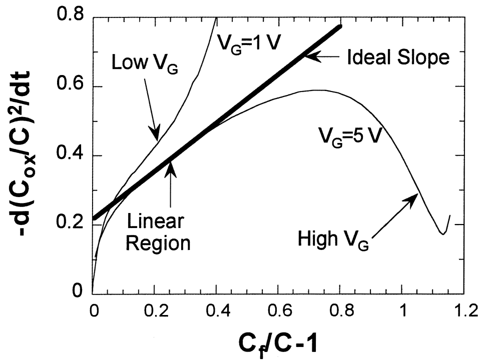

Fig. 1. Measured Zerbst plot of a p/p$^+$ epi wafer. The epi thickness is about 2.5 μm.

shown in Fig. 1, with τ_g inversely proportional to the slope of the Zerbst plot. This type of behavior is usually observed in bulk wafers. However, we typically see deviations from the ideal, when measuring epi wafers, as shown in Fig. 1. For low gate voltages with the scr width confined to the epi p-layer, the linear portion of the Zerbst plot is small and the slope is higher than for higher gate voltage leading to low τ_g. The second issue is the drop-off region with negative slope at high gate voltage, not observed in uniformly doped bulk wafers. The third issue is the effect of the p/p$^+$ interface. It is well known that there can be misfit dislocations at the interface because of lattice mismatch [6, 7]. We have characterized the epi layer through measurement and simulation to understand the various deviations from ideality.

2. The drop-off region of the Zerbst plot

The well known Zerbst equation is [2]

$$-\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{C_{\mathrm{ox}}}{C}\right)^2=\frac{2n_{\mathrm{i}}}{\tau_{\mathrm{g,eff}}N_{\mathrm{A}}}\frac{C_{\mathrm{ox}}}{C_{\mathrm{f}}}\left(\frac{C_{\mathrm{f}}}{C}-1\right)+\frac{K_{\mathrm{ox}}}{K_{\mathrm{s}}}\frac{2n_{\mathrm{i}}s_{\mathrm{eff}}}{t_{\mathrm{ox}}N_{\mathrm{A}}} \quad (1)$$

where C_{ox} is the oxide capacitance, t the time, C the measured capacitance, n_i the intrinsic carrier density,

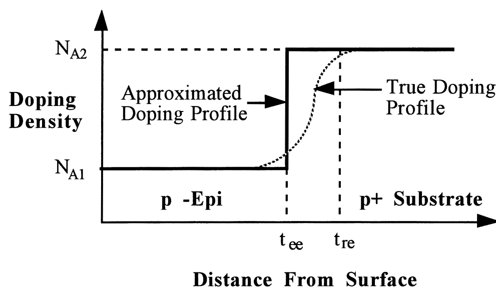

Fig. 2. Approximated and true doping profile of a p/p$^+$ epi wafer.

$\tau_{g,eff}$ the effective generation lifetime, N_A the doping density, C_f the measured final capacitance, K_{ox} the oxide dielectric constant, K_s the silicon dielectric constant, t_{ox} the oxide thickness and s_{eff} the effective surface generation velocity.

Generally, N_A, $\tau_{g,eff}$ and s_{eff} are considered constant in Eq. (1). If that is not the case, then it is difficult to obtain a linear portion in the Zerbst plot. One analysis used a non-linear $\tau_{g,eff}$ in constant N_A epi wafers [8]. Another used Eq. (1) for epi wafer analysis on relatively thick (10 to 15 μm) epi wafers [9]. However, for thin epi layers, if we apply a low gate voltage to confine the scr width to the lightly doped epi layer, the linear portion in Zerbst plot is reduced and it is difficult to determine $\tau_{g,eff}$ and s_{eff}.

To analyze thin epi p/p$^+$ wafers, we consider the effective doping-epi thickness of Fig. 2, where t_{re} is the true and t_{ee} the effective thickness for a step junction doping profile approximation. In our analysis t_{ee} is approximately the distance from the surface to a depth where the high doping density region starts.

The time rate of change of the inversion charge density is given as [2, 10]

$$\frac{\mathrm{d}Q_N}{\mathrm{d}t}=-\frac{qK_{\mathrm{s}}\varepsilon_{\mathrm{o}}N_{\mathrm{A2}}C_{\mathrm{ox}}}{C^3}\frac{\mathrm{d}C}{\mathrm{d}t} \quad (2)$$

A more detailed derivation of Eq. (2) is given in Appendix A. For uniformly doped wafers, $\mathrm{d}Q_N/\mathrm{d}t$ is similar to Eq. (2) with N_{A2} replaced by N_A. One may wonder why there is no N_{A1} term in Eq. (2). It is there but it is contained implicitly in the capacitance C, as seen in Eq. (A.10). The modified Zerbst equation for the epi/substrate case is

$$-\frac{\mathrm{d}(C_{\mathrm{ox}}/C)^2}{\mathrm{d}t}=\frac{2n_{\mathrm{i}}}{N_{\mathrm{A2}}\tau_{\mathrm{g,eff}}}\frac{C_{\mathrm{ox}}}{C_{\mathrm{f}}}\left(\frac{C_{\mathrm{f}}}{C}-1\right)+\frac{K_{\mathrm{ox}}}{K_{\mathrm{s}}}\frac{2n_{\mathrm{i}}s_{\mathrm{eff}}}{t_{\mathrm{ox}}N_{\mathrm{A2}}} \quad (3)$$

The measured C–t and resulting Zerbst plots of epi wafers are shown in Figs. 3 and 4, respectively. The C–t curves exhibit the expected behavior for $V_G \leq 3$ V. Beyond that, a flat portion develops during the early portion of the decay. That occurs when the scr region punches through to the p$^+$ substrate. Once the scr begins to collapse with time and is confined to the epi layer, the curves follow the "normal" C–t behavior. That is seen best by shifting the "$V_G = 3$ V" curve horizontally to the "$V_G = 9$ V" curve. Note the excellent coincidence between the two curves. In Fig. 3, the C–t curve for $V_G = 9.0$ V coincides with the C–t trace for $V_G = 3.0$ V when we shift the time axis of the latter curve by 826 s. Hence, in order to obtain reasonable $\tau_{g,eff}$ and s_{eff} values in thin epi wafers, it is necessary to apply sufficiently high gate voltages to drive the scr beyond t_{ee}.

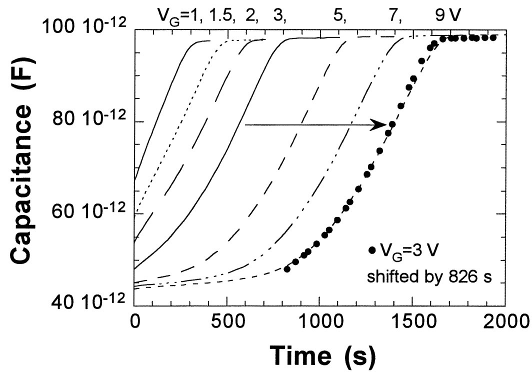

Fig. 3. Capacitance vs time for different gate voltages. By shifting the time axis by 826 s, the $V_G = 3.0$ V and $V_G = 9.0$ V curves overlap.

For the Zerbst plot in Fig. 4, generated with Eq. (1), we observe the following. First, the linear portion of the Zerbst plot is small for low gate voltages and it is difficult to obtain true $\tau_{g,eff}$ and s_{eff}. Second, as the gate voltage increases, the linear portion also increases but then saturates for $V_G > 3.0$ V. In fact, the Zerbst plot drops off with negative slope and the drop off increases for $V_G > 3.0$ V.

To confirm this type of behavior we have modeled this structure. The results, shown in Fig. 5, agree quite well with the experimental data. However, by increasing the gate voltage, a drop-off region is observed and increases as the gate voltage increases. We rewrite the Zerbst equation as

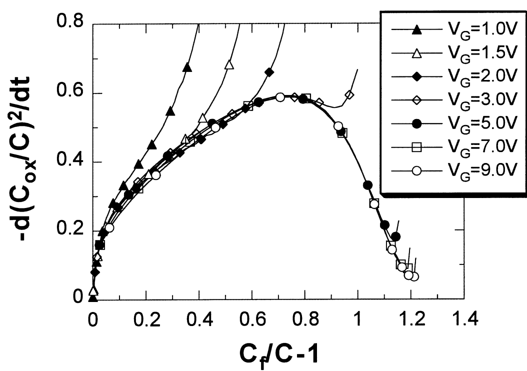

Fig. 4. Zerbst plots for different gate voltages, calculated from the data in Fig. 3 with Eq. (1). For $V_G = 1.0$ and 1.5 V, the small linear portion of the Zerbst plot makes it difficult to find $\tau_{g,eff}$ and s_{eff}. For $V_G > 3.0$ V, the linear portion is sufficiently large to determine $\tau_{g,eff}$ and s_{eff}. The drop-off region increases with higher V_G and the curves overlap.

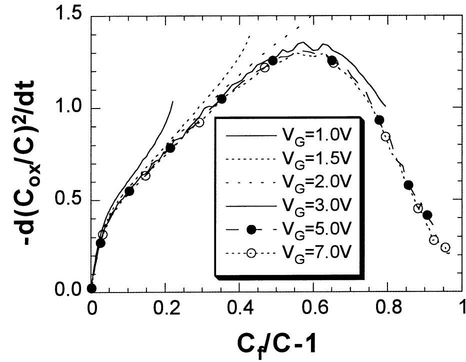

Fig. 5. Simulated Zerbst plots.

$$N_A = \frac{2n_i}{\tau_{g,eff}} \frac{1}{-d[(C_{ox}/C)^2]/dt} \frac{C_{ox}}{C_f}\left(\frac{C_f}{C} - 1\right) + \frac{2K_{ox}n_i s_{eff}}{K_s t_{ox}} \frac{1}{-d[(C_{ox}/C)^2]/dt} \quad (4)$$

This equation allows determination of N_A from a Zerbst plot, which is rarely done. To confirm the accuracy of Eq. (4), we measured the doping profile with the pulsed C–V method and compared it with that derived with Eq. (4) as shown in Fig. 6. The agreement between the two is quite good. Next, we used the doping profile obtained with Eq. (4) assuming $\tau_{g,eff}$ and s_{eff} to be constant, calculated the Zerbst plot and compared with experimental data, as illustrated in Fig. 6. The small discrepancy between the two may be due to some uncertainty in $\tau_{g,eff}$, s_{eff}, gate area and N_A. The $\tau_{g,eff}$ and s_{eff} are extracted from the linear portion of the Zerbst plot for $V_G = 7.0$ V and they are about 200 μs and 0.06 cm/s. Note from Fig. 6 that the Zerbst plot changes slope from positive to negative when N_A begins to increase and the scr punches into the p^+ substrate.

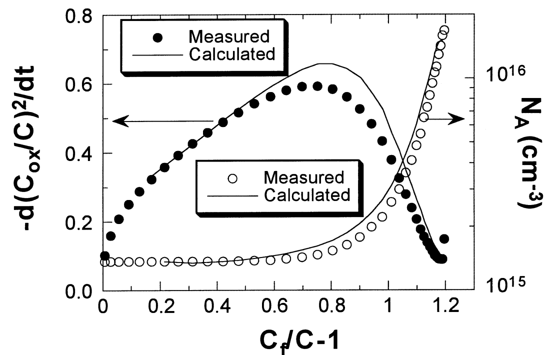

Fig. 6. Measured and calculated Zerbst and doping density plots for $V_G = 7.0$ V.

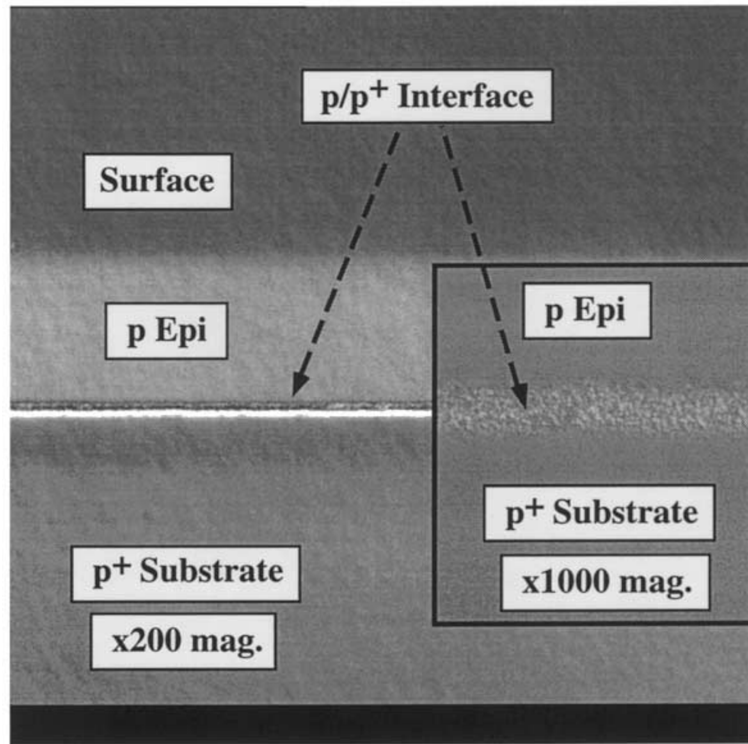

Fig. 7. The p/p $^+$ epi wafer, beveled at a 1°9′ angle and Wright etched for 15 s. The magnification is 200 ×. There appear to be no dislocation loops propagating from the p/p $^+$ interface into the epi layer.

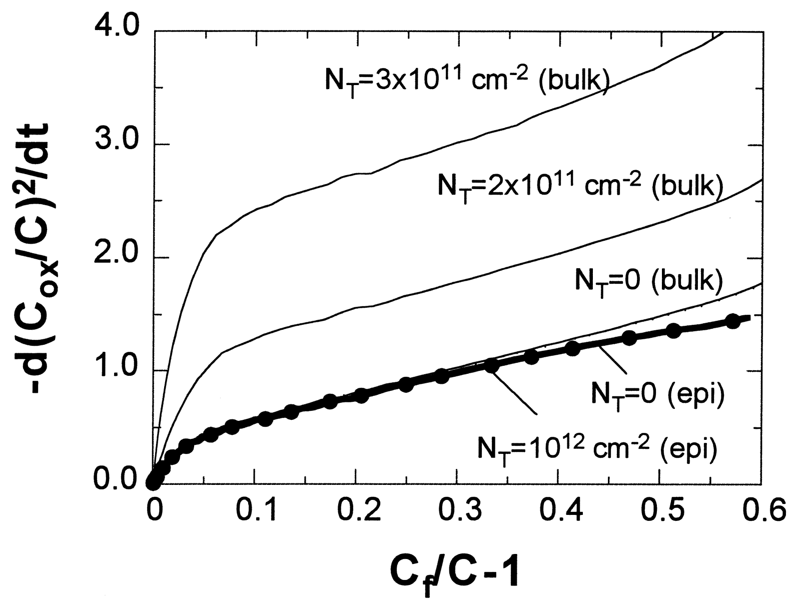

Fig. 8. Simulated Zerbst plots for bulk and epi. Bulk and epi: the traps N_T are located 2.5 μm from the surface. As N_T increases, s_{eff} increases, but $\tau_{g,eff}$ remains constant for bulk, while s_{eff} and $\tau_{g,eff}$ remain constant for epi samples.

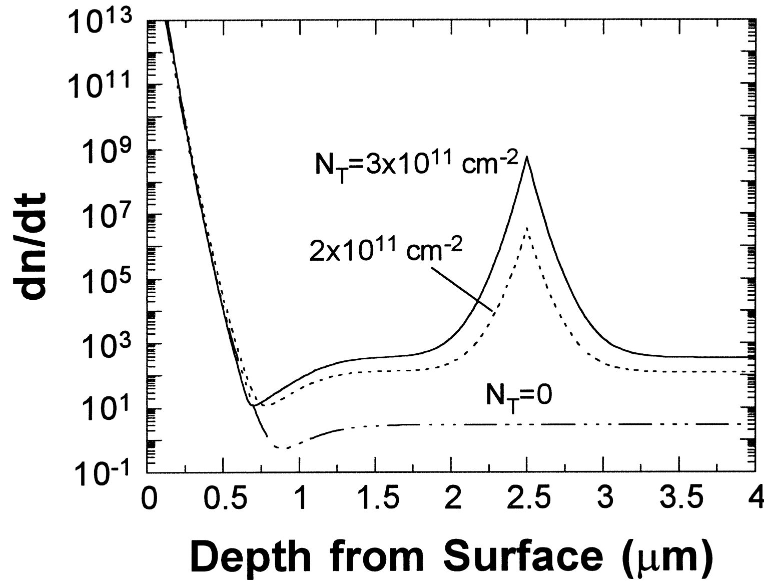

Fig. 9. Simulated electron generation rate, $\Delta n/\Delta t$, for $C_f/C-1 = 0.2$. The traps are located 2.5 μm from the surface.

3. Effect of the p/p$^+$ interface on generation lifetime

The p/p$^+$ interface may contain defects due to lattice mismatch between the p and the p$^+$ regions or native oxide residue before epi growth [11]. If the imperfect interface extends to t_{ee}, then dislocation loops or other defects can cause a nonlinear slope in the Zerbst plot because $\tau_{g,eff}$ is no longer constant. We assumed $\tau_{g,eff}$ constant in our calculations, giving a good fit with the measured data. Hence, we can say that there are few if any defects in this sample. We also checked for dislocation loops with Wright etching shown in Fig. 7. No dislocation loops were observed.

If imperfections are localized near the p/p$^+$ interface, then, to first order, they can be treated as a sheet of traps of density N_T. We simulated the effect of such traps on generation lifetime in bulk and in p/p$^+$ epi wafers. The results are shown in Fig. 8. These plots show that in uniformly-doped bulk wafers, s_{eff} (inversely proportional to the y-axis intercept) increases as N_T increases, but $\tau_{g,eff}$ (proportional to the slope) remains constant, as one would expect. However, in p/p$^+$ epi wafers, as N_T increases, both s_{eff} and $\tau_{g,eff}$ remain constant.

This constancy can be explained with the s_{eff} expression in Eq. (6) for $L < t_{bulk}$.

$$s_{eff} = s + \frac{n_i D}{N_A L} = s + \frac{n_i D}{N_A \sqrt{D\tau_r}} \tag{6}$$

where D is the diffusion constant, L the minority carrier diffusion length and τ_r the recombination lifetime. In bulk wafers, as N_T increases, τ_r in the substrate decreases and s_{eff} increases, causing the y-axis intercept in the Zerbst plot to increase. However, in the epi wafers, the substrate doping density is much higher, typically 10^4 times, than the epi doping density. Hence, the effect of reduced τ_r is negligible, even if there are interface traps at the p/p$^+$ interface.

The electron generation rate, $\Delta n/\Delta t$, in the bulk wafer determined from MEDICI simulations, is shown in Fig. 9. The trap density sheet is a substantial generation source. For N_T above 3×10^{11} cm^{-2}, the traps affect generation in the space-charge region and the Zerbst plot becomes non-linear. This is illustrated in Fig. 8 where for the bulk wafer at $C_f/C-1 \approx 0.4$–0.55, the slope increases beyond that in the 0.1 and 0.3 region.

4. Analysis of higher Zerbst slope for small gate voltages

It is well known that the Zerbst plot slope should remain independent of the gate voltage [12]. However, we have found that for low gate voltages, the slope of the Zerbst plot increases as shown in Fig. 4, regardless of wafer type. This may be the result of localized defects, localized doping density variations near the surface, improper data analysis and so on. To check these possibilities, we simulated bulk wafers as shown in Fig. 10. At the higher gate voltages, the slope is in fact constant, but at the lower voltages, it does depend

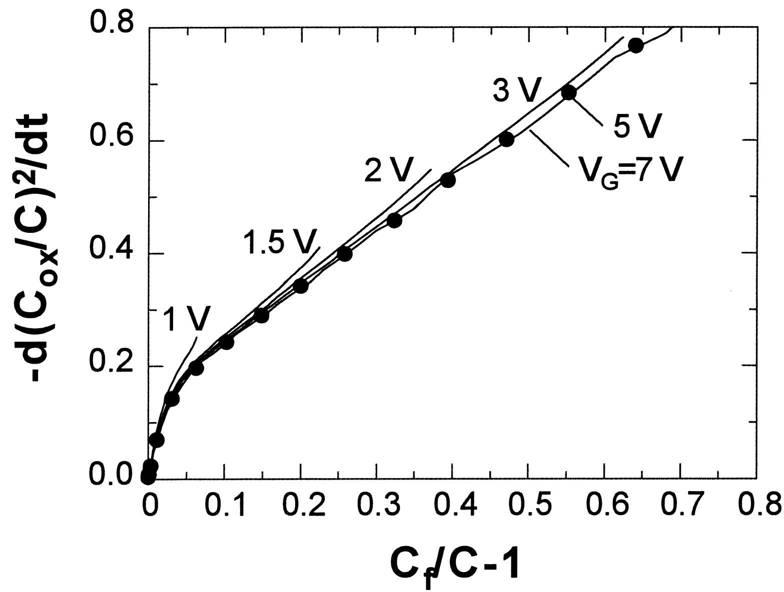

Fig. 10. Simulated bulk wafer Zerbst plots.

on the gate voltage, even though the doping density and lifetime are kept constant in this simulation. One possibility is an improper analysis with the chosen generation width W_g. It is well known that the conventional $W_g = W - W_f$ underestimates the generation width. Here W is the space-charge region width and W_f is the final scr width. Using the more accurate generation width $W_g = \sqrt{W^2 - W_f^2/2} - W_f/\sqrt{2}$ of Rabbani [13], we replot Fig. 4 in Fig. 11, but the higher slope at low gate voltages remains unchanged.

Fig. 11 shows that the increased low-voltage slopes are not the result of an incorrect generation width. Next we checked for the effect of interface traps, N_{it}, on the Zerbst plot shape, since the surface generation

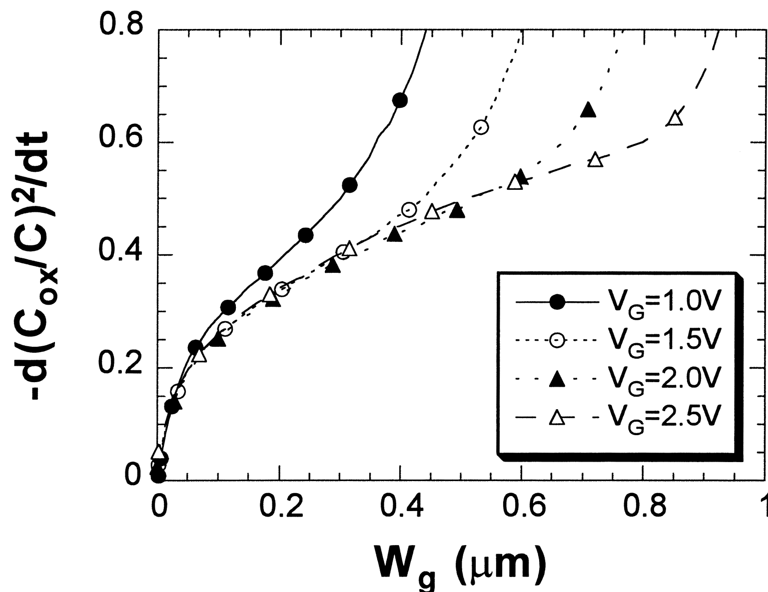

Fig. 11. Experimental Zerbst plot for an epi wafer for $V_G \leq 2.5$ V. This figure is replotted from Fig. 4 using Rabbani's generation width.

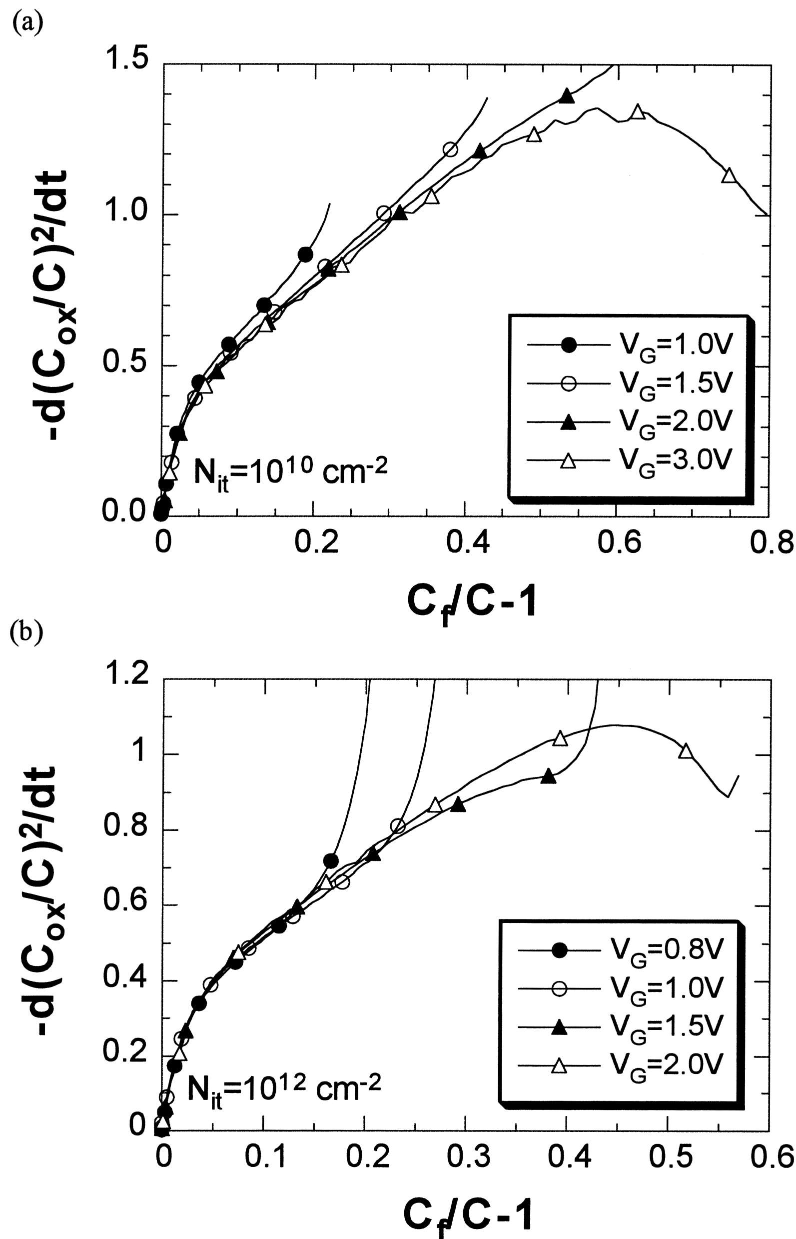

Fig. 12. Simulated epi wafer Zerbst plot for (a) $N_{it} = 10^{10}\ cm^{-2}$ and (b) $N_{it} = 10^{12}\ cm^{-2}$.

rate depends on interface traps [2]. We simulated Zerbst plots for epi wafers for $N_{it} = 10^{10}\ cm^{-2}$ in Fig. 12(a) and for $N_{it} = 10^{12}\ cm^{-2}$ in Fig. 12(b).

The higher slopes at low gate voltages disappear in Fig. 12(b), indicating that the higher slopes are likely due to interface generation. At low gate voltages, the generated carriers are insufficient to shield the surface from the scr region for low generation rates and $\tau_{g,eff}$ in the scr is affected by surface generation. For the higher N_{it}, however, the higher interface generation leads to enhanced surface shielding and the Zerbst slope at small gate voltages remains constant, because it is determined by bulk, not interface, properties. A similar explanation can be found in Fig. 8 for $N_T = 3 \times 10^{11}\ cm^{-2}$, where the slope for $0.4 \leq (C_f/C - 1) \leq 0.55$ is higher than that for $0.2 \leq (C_f/C - 1) \leq 0.4$ because of the effect of high N_T in the substrate.

5. Conclusions

We have extended the Zerbst theory and measurement to evaluate the lifetime and doping density of p/p$^+$ epi wafers. For thin epi layers, it is difficult to obtain a linear portion of the Zerbst plot because, at small gate voltages, the linear portion is small and the slope of the Zerbst plot increases. By applying a sufficiently high gate voltage which extends the scr to the p$^+$ region, we obtain a relatively broad linear region in the Zerbst plot and we also obtain the doping profile at the same time. The drop off region in the Zerbst plot for scr width $> t_{ee}$ is due to the non-uniform doping profile near the p/p$^+$ interface. Hence, the best way to obtain reliable generation lifetimes in p/p$^+$ thin epi wafers is to apply sufficiently high gate voltages. However, the main problem with pulsed MOS capacitors, is the long measurement time. We have already shown that the pulsed light method can solve this problem allowing $\tau_{g,eff}$ to be measured in a short time even for high gate voltages [14]. We also checked the effect of imperfect p/p$^+$ interfaces on the lifetime in the lightly doped epi layer. In p/p$^+$ epi wafer, the effect is too small to be observed because of the high substrate doping density.

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Appendix A

The gate voltage in MOS capacitors is

$$V_G - V_{FB} = \phi_s + V_{ox} \quad (A.1)$$

where V_{FB} is the flatband voltage, ϕ_s the surface potential and V_{ox} the voltage drop in the oxide, given by

$$V_{ox} = -\frac{Q_N - q\int_0^W N_A(x)\,dx}{C_{ox}} \approx -\frac{Q_N - qN_{A1}t_{ee} - qN_{A2}(W - t_{ee})}{C_{ox}} \quad (A.2)$$

where N_{A1} and N_{A2} are doping densities of the lightly doped epi layer and the heavily doped substrate, respectively. Eq. (A.2) is valid when the gate voltage is high enough for the scr to reach t_{ee} in the step junction approximation. If the scr is confined to the lightly doped epi layer, then Eq. (A.2) becomes $V_{ox} = (Q_N - qN_{A1}W)/C_{ox}$. The surface potential is usually $\phi_s = qN_A W^2/2K_s\varepsilon_o$. However, in our case

$$\phi_s = \frac{q(N_{A1} - N_{A2})t_{ee}^2}{2K_s\varepsilon_o} + \frac{qN_{A2}W^2}{2K_s\varepsilon_o} \quad (A.3)$$

From Eq. (A.3), we solve for W as

$$W = \sqrt{\frac{2K_s\varepsilon_o}{qN_{A2}}\left(\phi_s - \frac{q(N_{A1} - N_{A2})t_{ee}^2}{2K_s\varepsilon_o}\right)} \quad (A.4)$$

Substituting for W into Eq. (A.1), gives

$$V_G'' = V_G - V_{FB} + \frac{Q_N}{C_{ox}} = \phi_s + \frac{qN_{A1}t_{ee}}{C_{ox}} - \frac{qN_{A2}t_{ee}}{C_{ox}} + \sqrt{\frac{2qK_s\varepsilon_o N_{A2}}{C_{ox}^2}\left(\phi_s - \frac{q(N_{A1} - N_{A2})t_{ee}^2}{2K_s\varepsilon_o}\right)} \quad (A.5)$$

We can simplify Eq. (A.5) to

$$V_G'' = \phi_s + V_1 - V_2 + \sqrt{2V_{02}\phi_s - V_2^2\frac{(N_{A1} - N_{A2})}{N_{A2}}} \quad (A.6)$$

where $V_1 = qN_{A1}t_{ee}/C_{ox}$ and $V_2 = qN_{A2}t_{ee}/C_{ox}$. Solving for ϕ_s gives

$$\phi_s = V_G'' - V_{12} - V_{02} \times \left(\sqrt{1 + \frac{2(V_G'' - V_{12})}{V_{02}} - \left(\frac{V_2}{V_{02}}\right)^2\frac{(N_{A1} - N_{A2})}{N_{A2}}} - 1\right) \quad (A.7)$$

where $V_{01} = qK_s\varepsilon_o N_{A1}/C_{ox}^2$, $V_{02} = qK_s\varepsilon_o N_{A2}/C_{ox}^2$ and $V_{12} = V_1 - V_2$. Eq. (A.7) allows us to calculate the scr width W by substituting ϕ_s into Eq. (A.2), giving

$$W = \left(\frac{K_s t_{ox}}{K_{ox}}\right) \times \left(\sqrt{1 + \frac{2(V_G'' - V_{12})}{V_{02}} - \left(\frac{V_2}{V_{02}}\right)^2\frac{(N_{A1} - N_{A2})}{N_{A2}}} - 1\right) \quad (A.8)$$

The MOS capacitance expression for deep depletion is

$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_B}\right)^{-1} \quad (A.9)$$

where $C_B = K_s\varepsilon_o/W$ is the bulk scr capacitance. We substitute Eq. (A.8) into Eq. (A.9) and the MOS capacitance becomes

$$C = \frac{C_{ox}}{\sqrt{1 + (2(V_G'' - V_{12})/V_{02}) - (V_2/V_{02})^2((N_{A1} - N_{A2})/N_{A2})}} \tag{A.10}$$

This expression is valid only in the deep-depletion regime of the device. Solving Eq. (A.10) for V_G'', gives

$$V_G'' - V_{12} = \frac{V_{02}}{2}\frac{C_{ox}^2}{C^2} - \frac{V_{02}}{2} + \frac{V_{02}}{2}\left(\frac{V_2}{V_{02}}\right)^2 \frac{(N_{A1} - N_{A2})}{N_{A2}} \tag{A.11}$$

Differentiating Eq. (A.11) with respect to time, the second and the third term on the right hand side of Eq. (A.11) will be zero because they are constant. Then Eq. (A.11) becomes

$$\frac{dV_G}{dt} = \frac{dV_{FB}}{dt} - \frac{1}{C_{ox}}\frac{dQ_N}{dt} - V_{02}C_{ox}^2\frac{1}{C^3}\frac{dC}{dt} \tag{A.12}$$

If V_G is constant, dV_G/dt is zero and dV_{FB}/dt is also zero because V_{FB} is constant. Then Eq. (A.12) becomes

$$\frac{dQ_N}{dt} = -\frac{qK_s\varepsilon_o N_{A2} C_{ox}}{C^3}\frac{dC}{dt} \tag{A.13}$$

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