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Abnormal transconductance and transient effects in partially depleted SOI MOSFETs

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Abstract

A transconductance dip, observed in floating body partially depleted SOI devices, is due to transient effects and is reduced with a positive back bias in SOI nMOSFETs. MEDICI simulations show that both hole and electron densities near the front interface fluctuate during the turn-on transient, causing a small decrease and then an increase of the drain current that leads to the transconductance dip. Transient effects also cause an initial current ramp in I_{DS}–V_{GS} characteristics at the start of the gate voltage sweep when the back gate is inverted. The transient effect diminishes as the channel length and channel width decrease and as the back bias increases.

1. Introduction

Silicon-on-insulator (SOI) technology has a number of advantages over traditional bulk CMOS technology [1]. As the dimensions of MOS transistors shrink, problems such as creating shallow junctions, CMOS latch-up, higher leakage current, and higher parasitic capacitances are difficult to solve in traditional bulk CMOS technology. SOI technology, on the other hand, offers solutions to these problems and is ideal for low-power applications [2].

Due to the existence of the floating body in partially depleted SOI devices, transient effects are significant when the body is not tied to a fixed voltage [3–8]. The drain current experiences a long transient delay before reaching a stable value, thus influencing the drain current just after gate switching and in steady-state. This subsequently causes different subthreshold slope and threshold voltage.

Shin et al. described a simple one-dimensional analytical model which quantitatively predicts the impact of the floating body on the drain current transient in partially depleted TFSOI devices [9]. The "apparent" threshold voltage measured immediately after the gate voltage is applied is about 94 mV less than the steady-state value in partially depleted SOI devices. This is important for short measurement times. The transient characteristic is a measure of the quality of the SOI material.

Gautier et al. emphasized the role of the overall hole charge in the body of the device, and their result demonstrated drain current overshoot, undershoot, memory effects, and dynamic instabilities in submicron partially depleted devices [3]. They reported that transient effects influence the drain characteristics. Large drain current differences exist between steady state and the beginning of gate switching.

Drain current transients in a partially depleted floating body SOI device can affect the circuit operation in various ways. The circuit may not behave similarly under different frequencies [10, 11]. The transient overshoot was modeled analytically by Lim [12] and can be beneficial in low-voltage circuits. Wei reported that the drain current transient is due to slow body-charging transients [13], and this transient does not happen in fully-depleted SOI transistors.

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The transient effect can be reduced by tying the body to a fixed potential, such as the source. However, the additional drain current due to the transient effect is lost. This additional current can be used in digital circuits to boost the current drive capability.

In this paper, SOI transient effects were simulated with MEDICI [14]. The results show the hole and electron densities to fluctuate during the turn-on transient, causing a small change in the drain current, leading to a dip in the transconductance. Experimental results also show this transconductance dip. With increased back bias, the dip is reduced, because the neutral floating body region is reduced. The transient effect, related to the floating body, is also reduced.

2. Floating body transient effects

Due to the capacitance coupling between the front gate and the floating body, switching of the front gate voltage changes the body potential momentarily. If the body of a partially depleted SOI device is not tied to a fixed potential, carriers need to be generated or recombine through the front and back interfaces as well as through the p–n junctions in order to reach steady state. This may take several seconds. Before carriers are generated or recombine, the potential is lower or higher than its final value, resulting in a change of threshold voltage and drain current.

As time elapses during the turn-off transient, holes are generated and the potential in the device rises. The drain current, therefore, will also rise from a low value to its final, stable value. During the turn-on transient, holes recombine, and the potential is high initially and then returns to its final, stable value. Thus the drain current experiences a high to low transition. The turn-off transient delay is usually longer than the turn-on transient delay [15].

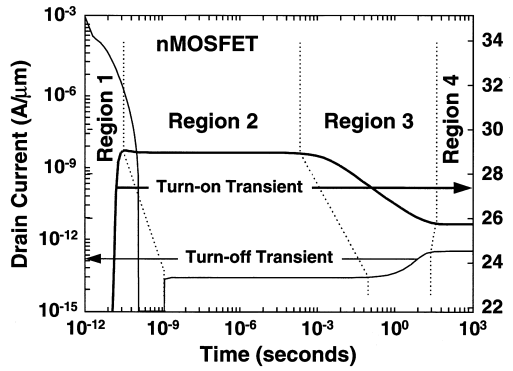

Fig. 1. Four regions during SOI turn-off and turn-on transients.

When the front gate voltage is switched from a high gate voltage to a low gate voltage in partially depleted SOI nMOSFETs, the floating body potential changes from a high value to a low value quickly, resulting in an increase of the threshold voltage and a decrease of the drain current, as shown in Fig. 1. With time, the body potential rises and the threshold voltage decreases. Eventually, the drain current reaches steady-state. Therefore, the turn-off transient suppresses the off-state drain current. We divide the turn-off transient into four regions, as shown in Fig. 1; region 1: drain current drops sharply; region 2: drain current remains low; region 3: drain current rises; region 4: drain current attains steady state.

When the gate voltage is changed from low to high in partially depleted nMOSFETs, the floating body potential changes from a low value to a high value initially, causing a threshold voltage decrease and a drain current increase. The drain current returns to its final value after some delay. Hence, the turn-on transient enhances the on-state drain current. Similar to the turn-off transient, the turn-on transient can be divided into four regions, as shown in Fig. 1; region 1: drain current increases sharply; region 2: drain current remains high; region 3: drain current drops; region 4: drain current attains steady state. These four regions will be used in the following sections to compare the change of the potential, hole and electron densities at various times.

In this paper, partially depleted SOI transistors were fabricated on SIMOX wafers. The gate oxide thickness is 100 Å, the buried oxide thickness is 3500 Å, the silicon film thickness is 1000 Å, and the doping density is about $2 \times 10^{17}\,\mathrm{cm}^{-3}$. Devices with channel lengths from 0.4 to 25 μm, and channel widths from 0.5 to 25 μm were made. Auger and Shockley–Read–Hall recombination models in MEDICI are used to simulate SOI transients.

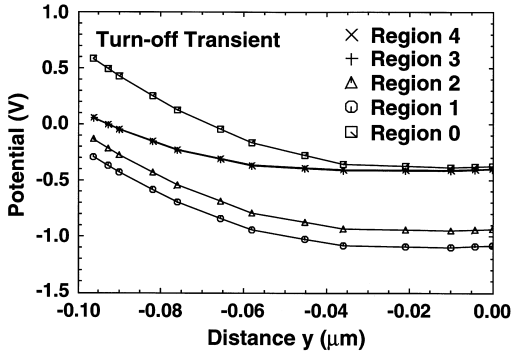

Fig. 2. Simulated potential distribution in a partially depleted SOI nMOSFET with its body floating during the turn-off transient. Region 0 is before gate switching.

3. Simulation

3.1. Potential distributions

In the following simulations, the $y = 0$ is the thin silicon/BOX interface, and the $y = -0.1$ μm is the thin silicon/gate oxide interface. The simulated potential distribution in a partially depleted SOI nMOSFET during the turn-off transient is shown in Fig. 2. The initial V_{GS} is 2 V, and is switched to 0 V at 10^{-12} s. The V_{DS} is 0.1 V. Before gate switching (region 0), the SOI device is *on*. The front gate interface is heavily inverted and the surface potential is *high*. Just after the turn-off transient, the surface and the body potentials suddenly decrease, as shown in region 1 in Fig. 2. The potential drop near the front gate interface is slightly higher than that in the body. The potential near the surface and the potential in the body then start to rise. From region 1 to region 2, the surface potential and the body potential rise at about the same rate. They reach their final values after region 3. The potential at the back interface increases more than that near the front gate interface. In addition, the back surface potential in region 4 is close to that in region 0.

During simulation of the turn-on transient, the body potential changes from a low value to a high value just after gate switching, and then returns to its initial low value, as shown in Fig. 3. The V_{GS} is switched from 0 to 2 V at 10^{-12} s. The V_{DS} is fixed at 0.1 V. From region 0 to region 1, the front surface potential suddenly increases from a low value (front gate depletion) to a high value (front gate inversion). Again the potential increase at the front surface is slightly higher than at the back surface. It is interesting to note that the surface potential in region 1 is much higher than its steady state value in region 4. After region 1, the surface potential starts to drop. It reaches its final value in region 2, with the front interface strongly inverted.

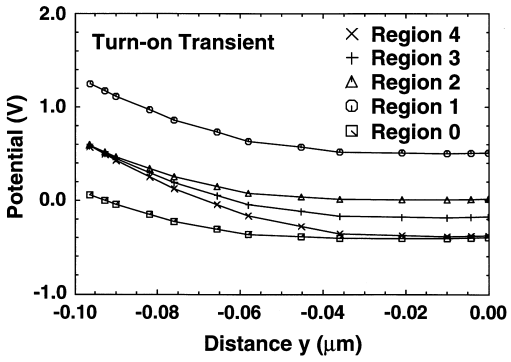

Fig. 3. Simulated potential distribution in a partially depleted SOI nMOSFET with its body floating during the turn-on transient. Region 0 is before gate switching.

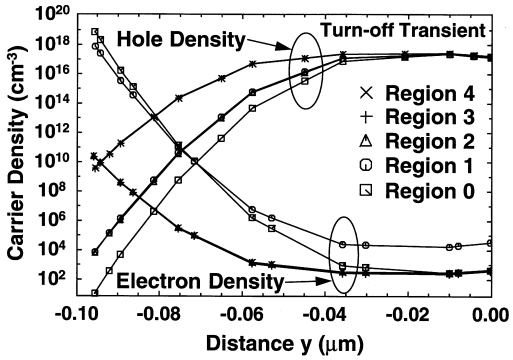

Fig. 4. Simulated hole and electron densities in a partially depleted SOI nMOSFET with its body floating during the turn-off transient. Region 0 is before gate switching.

The potential at the back interface, however, continues to drop until region 4, when the back surface potential returns to a value that is about the same as that in region 0.

3.2. Hole and electron densities

Fig. 4 shows the distribution of hole and electron densities in an SOI nMOSFET during the turn-off transient. Before the turn-off transient (region 0), the hole density is *high* in the body and *low* towards the surface due to the inversion at the front interface. The hole density in the body does not change during the turn-off transient, but near the surface it increases significantly from region 0 to region 4. The electron density in the body rises slightly from region 0 to region 1, and returns to its initial value in region 2. The electron density near the surface decreases slightly from region 0 to region 1, but drops quickly to a final, low value in region 2.

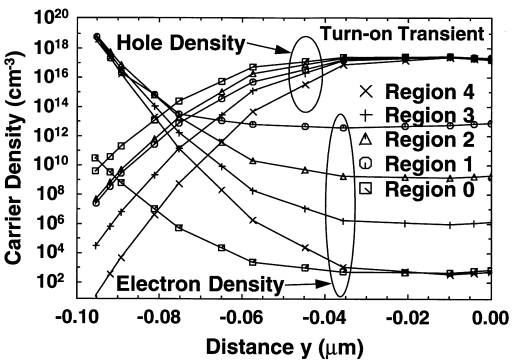

Fig. 5. Simulated hole and electron densities in a partially depleted SOI nMOSFET with its body floating during the turn-on transient. Region 0 is before gate switching.

The hole density in the body (close to the back surface) does not change much during the turn-on transient, as shown in Fig. 5. The hole density near the surface, however, reduces from region 0 to region 1, increases slightly from region 1 to region 2, and then continues to drop, up to region 4. The electron density near surface changes from a low value in region 0 to a high value in region 1, quickly forming an inversion layer. The electron density in the body exhibits a large increase during this period. In region 2, the electron density near the surface continues to increase slightly, while the electron density in the body starts to drop. The electron density near the surface then drops in region 3, reaching steady state. The electron density in the body continues to drop until region 4. The high electron density near the front surface and in the body contributes to the drain current increase during the turn-on transient.

Hence, during the turn-off transient, holes are generated, resulting in a higher hole density near the surface, as shown in Fig. 4, region 4. During the turn-on transient, on the other hand, holes recombine, resulting in a lower hole density near the surface, as shown in Fig. 5, region 4.

4. Experiments

4.1. Transient effects on transconductance

The SOI turn-on and turn-off transients are measured with an HP4145B semiconductor parameter analyzer using short integration time. For short integration times, the measured data are stored directly into memory and displayed on the screen. This is different from the normal gate or drain characteristic measurements, where medium or long integration times are normally preferred. Transient effects can influence the measured drain current, therefore affect the transconductance g_m. In our measurement, we noticed a g_m dip in the transconductance vs gate voltage curve in both partially depleted nMOSFETs and pMOSFETs. The g_m dips appear in both negative and zero back biases, but disappear at a positive back bias of 10 V in SOI nMOSFETs, with all other instrument setups remaining the same, as shown in Fig. 6. In SOI pMOSFETs, the g_m dips are shown at positive and zero back biases, but disappear for negative back bias. Therefore we believe that the g_m dips are not due to measurement artifacts.

The g_m dip is related to transient effects in partially depleted, floating body devices. As the gate voltage is stepped up in nMOSFET, a small voltage increase is applied to the gate each time, resulting in turn-on transients. According to Fig. 5, the hole density is lowered from region 0 to region 1. It rises slightly from region 1 to region 2, and then continues to drop, until it reaches steady state in region 4. Hence, there is a hole density fluctuation during the turn-on transient. The electron density in Fig. 5, on the other hand, starts from a low value in region 0, then increases from region 0 to region 1 suddenly just after gate switching. Near the surface, the electron density increases slightly from region 1 to region 2, and then starts to drop. In the body, the electron density decreases from region 1 to region 2. Again there is an electron density variation during the turn-on transient. The fluctuation of hole and electron densities causes a small decrease and then a small increase of the drain current. Although this drain current change is very small and can barely be

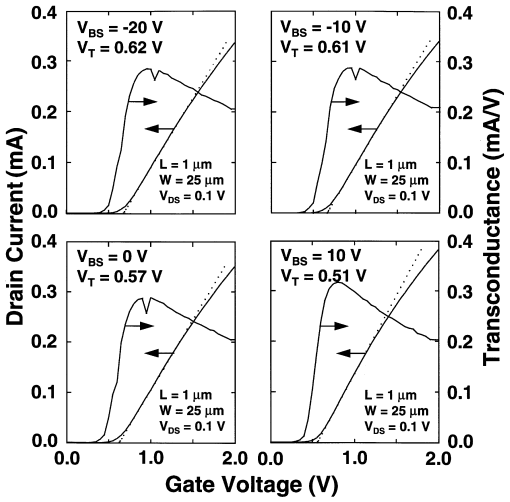

Fig. 6. Transconductance dip in a partially depleted SOI nMOSFET for different back biases.

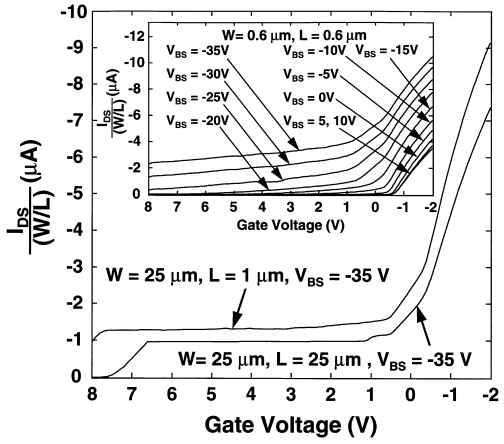

Fig. 7. Measured transient effects in $I_{DS}/(W/L)$–V_{GS} characteristics for different channel lengths and widths in SOI pMOSFETs. W/L = 25 μm/25 μm, 25 μm/1 μm, and 0.6 μm/0.6 μm.

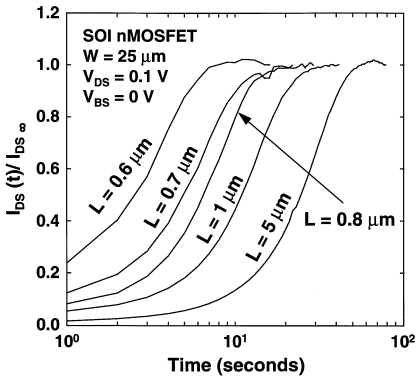

Fig. 8. Measured drain current turn-off transients for SOI nMOSFETs with channel lengths from 0.6 to 5 μm. $W = 25$ μm, $V_{DS} = 0.1$ V, and $V_{BS} = 0$ V. The drain current is normalized to the steady-state value.

noticed in the gate characteristics, it appears clearly in the transconductance plot.

The back interface in a partially depleted SOI device can be accumulated, depleted, and inverted by varying the back bias. Adding a positive back bias for an nMOSFET depletes the back interface, reducing the width of the neutral region of the floating body. The device behavior changes as the thickness of the neutral region reduces [15]. When a small positive back bias is applied to the medium thickness partially depleted nMOSFET, the back gate interface starts to deplete. If the device is *on* (a positive front gate voltage higher than the threshold voltage), the front interface is inverted, with a space-charge region (scr) width x_{dmax}. At a sufficiently high back bias, the two scr layers from the front interface and from the back interface merge. Under these conditions, the device becomes fully-depleted. Floating body effects, such as kink effects, are reduced. In addition, the drain current is increased and the threshold voltage is reduced. This explains the reduction of the transconductance dip as the back bias increases in the SOI nMOSFET in Fig. 6.

4.2. Device dimensions vs transient effects

Fig. 7 shows the relation between the device dimensions and the drain current transient at the beginning of the gate bias in the I_{DS}–V_{GS} characteristics. Due to an initial positive back bias on the SOI pMOSFET, the device experiences a turn-off transient. The drain current at a gate voltage of 8 V is lower at the start of the gate voltage sweep. It rises as the gate voltage reduces. Note that the x axis, which is the voltage in our measurements, is proportional to time. The initial drain current ramp at the start of the gate voltage sweep is due to the transient effect.

This kind of drain current transient is not noticeable in bulk devices where the transient effect is small. For partially depleted, floating body devices, the transient time is long, and thus the drain current ramp is apparent. By comparing the $W/L = 25$ μm/1 μm and $W/L = 25$ μm/25 μm devices, we see that the longer the channel length, the longer the transient time. For small SOI devices, such as a $W/L = 0.6$ μm/0.6 μm device, the transient effect is further reduced.

A set of turn-off experimental transient curves of partially depleted nMOSFETs with different channel lengths are shown in Fig. 8. Partially-depleted, long channel devices exhibit longer turn-off times. The transient delay appears to relate to the volume of the neutral region. As the channel length of the device reduces, the volume of the neutral region is reduced, and the overall floating body effect becomes less important.

Although the turn-off transient delay is longer than the turn-on transient delay, the turn-off transient is not important because the magnitude of drain current is very small. The higher drain current during the turn-on transient, on the other hand, does create some drain current non-uniformity during the large gate voltage transition. This may cause a problem for analog applications.

5. Conclusion

Abnormal transconductance due to transient effects is observed in partially depleted SOI MOSFETs. The transconductance dip is related to the change of the hole and electron densities during the turn-on transient, leading to a change of the drain current. In addition, the dip is reduced as a positive bias is applied to the back gate of SOI nMOSFETs. Experimental data of gate characteristics in partially depleted devices also show that at the beginning of the gate voltage sweep, the drain current exhibits a ramp. It reaches steady state after a few seconds. This current ramp is due to SOI transient effects, which reduces in small MOS devices.

Acknowledgements

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