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Nonvolatile memory disturbs due to gate and junction leakage currents

J.E. Park [a,b,*], J. Shields [c], D.K. Schroder [b]

[a] IBM Microelectronics, 2070 Route 52 2N6 445, Hopewell Junction, NY 12533, USA

[b] Department of Electrical Engineering and Center for Solid State Electronics Research, Arizona State University, Tempe, AZ 85287-5706, USA

[c] Microchip Technology, Tempe, AZ 85282, USA

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Abstract

We address *disturbs* due to gate oxide and junction leakage currents in floating gate nonvolatile memories (NVM). The junction leakage is important, because the gate oxide current is proportional to junction current. We find the low gate leakage current to be caused by field ionization (FI) from traps within the gate oxides. Such low gate leakage currents can lead to sufficient charge accumulation to disturb charge in the floating gate. Through detailed simulations and measurements, we have determined the main cause of "write disturb" and "erase disturb" to be FI gate oxide current at low electric fields and Fowler–Nordheim current at high electric fields. Additional currents are due to high-energy electrons from the junction leakage current.

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1. Introduction

Nonvolatile memories (NVM) function by storing charge on floating gates, which are charged and discharged by current flow through insulators. The properties of these insulators are, therefore, very important. Many insulator extrinsic defect and impurity densities have been reduced so that they face their intrinsic limitations such as Fowler–Nordheim (FN) and direct tunneling. However, "disturb" problems can become significant due to device scale-down and high packing density. Memory cells are usually connected to each other through common word and bit lines because complete cell isolation is impractical. Therefore "disturb" must be reduced and minimized. Any unintentional change of threshold voltage can be considered a "disturb", leading to erratic logic decisions. We address current "disturb" in this paper.

Leakage currents, which can be harmful to NVM, can be divided into junction and gate leakage currents. Energetic carriers, generated at the drain/source junction, contribute to the junction leakage current, which can be injected into the floating gate under high electric fields. This usually occurs during "write" and "erase" operations. At low electric fields, charge compensation is possible due to low gate leakage current, which increases as the gate oxide is stressed after "write" and "erase" as well as "read" cycles.

Although it is an extremely difficult task to have 10-year lifetime expectancy without suffering from serious "disturbs" after numerous "write" and "erase" as well as "read" operations, better device performance can be achieved by understanding the origins of "disturbs". In this paper, we present a detailed analysis of each "disturb" cause and its effect on NVMs. We find field-ionization (FI) currents to be a major gate leakage current at low electric fields. We also discuss junction leakage currents induced by stress due to LOCOS and trap-assisted tunneling (TAT).

* Corresponding author. Address: IBM Microelectronics, 2070 Route 52 2N6 445, Hopewell Junction, NY 12533, USA. Tel.: +1-845-894-4459.

E-mail address: parkje@us.ibm.com (J.E. Park).

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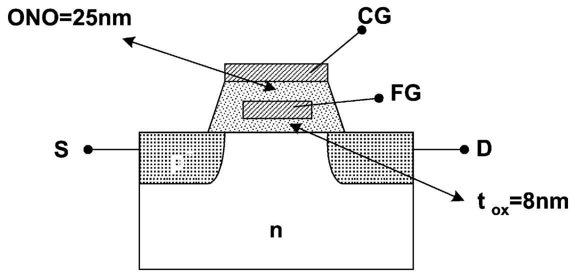

Fig. 1. Cross-section through the NVM of this paper.

2. Experimental

Our devices are p-channel NVMs with 8 nm gate oxides and oxide/nitride/oxide (ONO) between the floating and control gates. A schematic cross-section of the device is shown in Fig. 1. We had a test NVM structure with a floating-gate contact, which allowed us to monitor leakage currents through the gate oxide. Also two different sized diodes were fabricated using LOCOS in order to observe the mechanical stress effect on diode leakage current since the drain and source form the junction with the well or substrate.

3. Junction leakage current

We address junction leakage current first, because we found the control and floating gate leakage currents to be strongly correlated to junction leakage currents through experimental measurement, obvious at high electric fields, as shown in Fig. 2. The source and drain are reverse biased to junction breakdown and gate leakage current (I_G), which is the summation of FG and CG currents, is measured simultaneously. Although the gate currents is not shown below 10^{-14} A, it is clearly seen that it is proportional to the junction leakage current in the high reverse-biased voltage regime. At $T = 330$ K, the leakage currents are higher than they are at room temperature, because the gate current is related to the product of the tunneling probability and the number of available carriers with more carriers leading to higher gate leakage currents. Hence, reduction of junction leakage currents minimizes gate leakage currents. Junction leakage current is not only a function of temperature, but also depends on junction geometry. We measured the junction leakage current of diodes fabricated with LOCOS with are of about 10^{-4} cm^2 for the large diode and 3×10^{-8} cm^2 for the small diode. We find the leakage current density of the small diodes to be much higher than of the large diodes as shown in Fig. 3. In the following discussions, the three major causes of these high and abnormal leakage currents are pointed out.

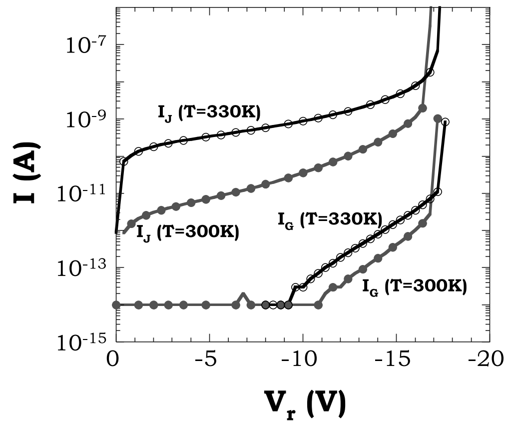

Fig. 2. Junction and gate leakage current versus junction reverse bias voltage as a function of temperature.

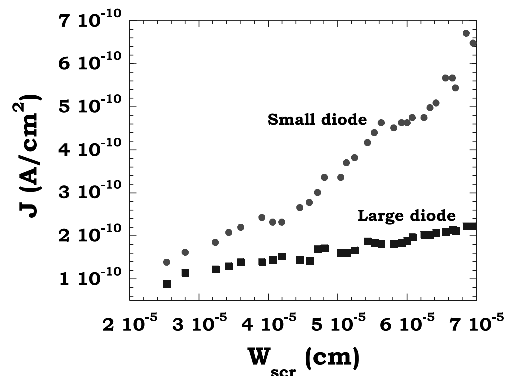

Fig. 3. Leakage current densities versus space-charge region width for small- and large-area diodes.

3.1. Stress generation for LOCOS processing

As a result of scaling, the diode perimeter becomes more important compared to the diode area and the internal stress of devices increases, leading to dislocations and oxide integrity degradation. The stress field near the nitride edge causes the generation of dislocations in the silicon along Si_3N_4 edges during LOCOS processing. For our study, p^+n diodes were fabricated in n-type wells on p-type substrates with LOCOS isolation. The pad SiO_2 thickness is 30 nm and the Si_3N_4 thickness is 160 nm.

The viscoelastic oxidation model of TSUPREM [1] was used to simulate the stress as shown in Fig. 4. The edges of the bird's beaks experience compressive stresses around hundreds of Mpa. Dislocations can be created at these stressed regions. According to Bohg and Gaind [2], the minimum pad oxide thickness without dislocation formations is about one third of that of Si_3N_4. There is a trade-off between the defect protection and lateral oxide

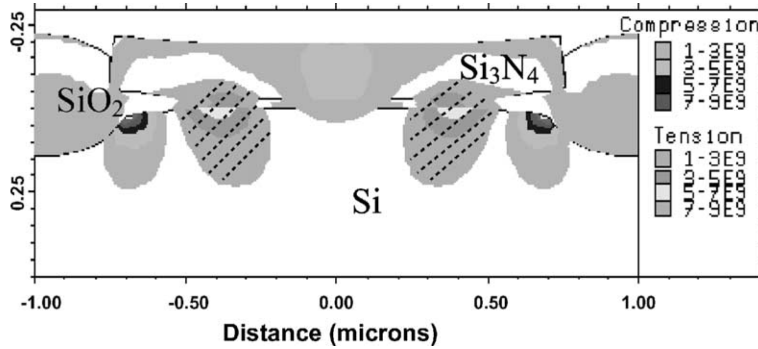

Fig. 4. LOCOS fabricated diode stress simulated with the viscoelastic oxidation model and the unit for the stress is in Pa. The areas under tension are shaded.

encroachment. A nitride to thermal pad oxide thickness ratio of 2.5:1 produces a lateral encroachment or bird's beak [3]. Compressive stress can form additional gettering sites for metallic contamination [4]. Furthermore the band gap of stressed Si is reduced and the intrinsic carrier density, n_i, is increased by the stress [5]. Under compressive stresses, the silicon band gap is decreased by 14 meV/Mpa according to Smeys et al. [5].

The leakage current density, J_r, of reverse-biased p^+n junctions is given by [6]

$$J_r = J_{scr} + J_{diff} = \frac{qn_i W}{\tau_g} + \frac{qn_i^2 D_p}{N_D L_p} \tag{1}$$

where J_{scr} is the space-charge region (scr) generation current component, J_{diff} the diffusion current component, W the space-charge region width, L_p the minority carrier diffusion length, D_p the minority carrier diffusion coefficient, N_D the doping density, and τ_g the generation lifetime. An increase of n_i, caused by the stress, implies an increase of leakage current because diffusion current and generation current components are proportional to n_i^2 and n_i, respectively.

Not only the stress but also higher electric field can develop around the curved junction area and the junction can easily reach breakdown. During NVM operation, high voltages are usually required for fast programming and erasing cells. These voltages can lead the junctions into the soft breakdown regime and create hot electrons and holes. Furthermore, hot carriers enhance the gate leakage current by stressing the gate oxide, which can alter the charges in the floating gate. The actual electric field distribution is not homogeneous over the entire junction area. Sze and Gibbons [7] studied the effect of the radius of curvature of the metallurgical junction extensively. Because the spherical region of the junction has higher electric field, it determines the avalanche breakdown.

We placed a diode under reverse-biased conditions and ramped up the voltage until breakdown was observed using photon emission microscope imaging (EMMI) shown in Fig. 5. In the picture, the upper right corner of the diode starts to emit photons generated by impact ionization. In the soft breakdown regime, the corner of the diode initially shows photon emission, which subsequently propagates along the sides at the higher electric field (hard breakdown). It shows that the electric field at the corner is the dominant factor for the leakage current behavior in the soft breakdown regime.

The potential contour plot was calculated using MEDICI, also showing that impact ionization occurs more severely at the edge of the junction in Fig. 6. One can observe the small circle shaped contours and narrow line spacing in the upper middle part of the figure corresponding to a high electric field. The small dashed lines represent the metallurgical junction between the p^+ region and the n substrate.

3.2. Trap-assisted tunneling

At soft breakdown, a high junction leakage current that may be due to metal precipitates flows at reverse voltages well below the avalanche breakdown voltage. High-field regions around these metallic precipitates cause excess leakage current and localized breakdown. Since SiO_2, especially at the interface with stressed Si, is a preferred gettering place for metallic contamination [4,8], precipitates can form along the LOCOS perimeter edge under stress. The traps are more active generation and recombination (G–R) centers leading to higher leakage current as the electric field increases.

At high electric fields, the emission of carriers can be enhanced by tunneling via traps [9,10], in addition to Shockley–Read–Hall (SRH) thermal emission [11]. The expression for TAT generation rate is given as [10]

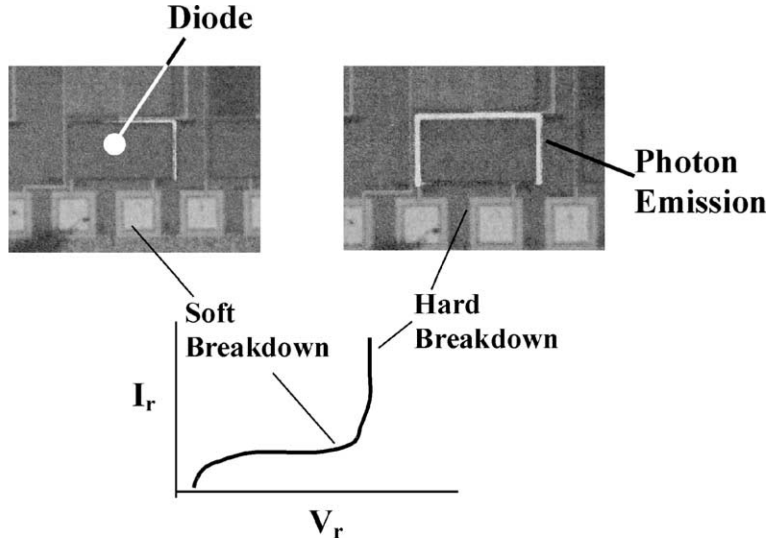

Fig. 5. EMMI pictures of a diode under high electric fields.

$$G_{TAT}(x) = (1 + \Gamma)G_{SRH}(x) \tag{2}$$

where

$$\Gamma = 2\sqrt{3\pi}\frac{|E_r|}{E_\Gamma}\exp\left(\frac{E_r}{E_\Gamma}\right)^2; \quad E_\Gamma = \frac{\sqrt{24m^*(kT)^3}}{q\hbar}$$

E_r is the localized electric field, G_{SRH} (x) is the spatial SRH expression, and m^* (taken as 0.25 m_0) is the effective mass.

The generation current with TAT, is given by

$$J_{scr} = q\int_0^W G_{TAT}(x)\,dx = q\int_0^W \frac{n_i(1+\Gamma)}{\tau_g}\,dx = \frac{qn_iW(1+\Gamma)}{\tau_g} \tag{3}$$

J_{scr} is calculated as a function of V_r and plotted in Fig. 7, taking the trap-assisted factor, Γ, and impact ionization into account. With the total leakage current being the product of impact ionization factor and junction leakage current due to carrier generation, small increases of leakage current by TAT generation are multiplied by impact ionization, but the difference in current between trap-assisted and conventional current diminishes as the multiplication factor M approaches infinity.

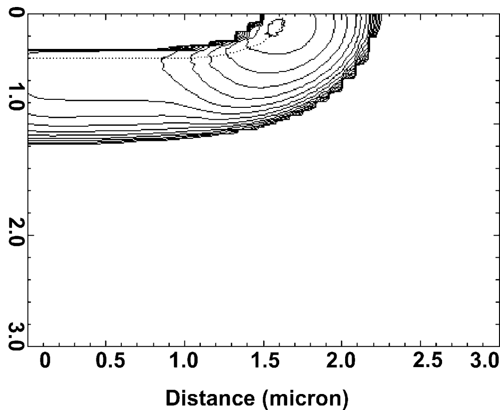

Fig. 6. Simulated electric field contour plot.

3.3. Total junction leakage current

The total junction leakage current consists of saturation, generation and surface components as well as a parasitic component, I_p. The total leakage current, I_r, can be expressed as

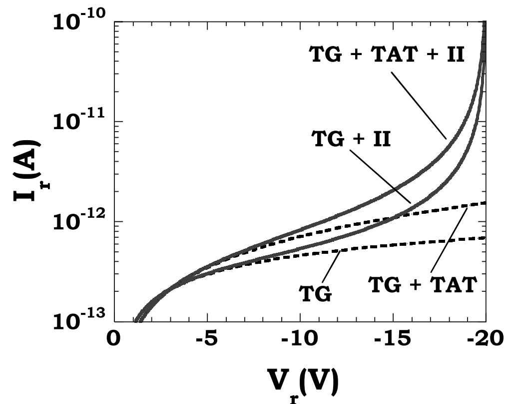

Fig. 7. Leakage current with and without trap-assisted tunneling. TG: thermal generation, TAT: trap-assisted tunneling, II: impact ionization.

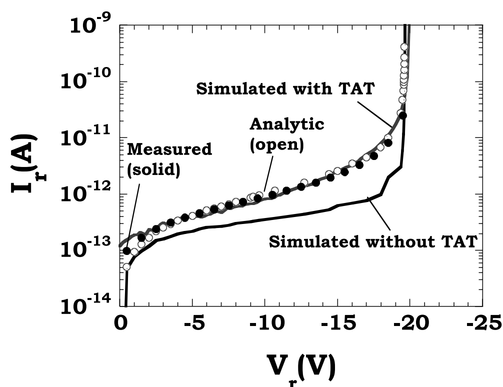

Fig. 8. Analytic, experimental and simulated leakage currents.

$$I_r = I_{scr} + I_{diff} + I_{sur} + I_{par} = \frac{qn_i W(1+\Gamma)A}{\tau_g} + \frac{qn_i^2 D_n A}{N_A L_n} + qn_i s_g A_s + I_{par} \quad (4)$$

The leakage current generated in a depleted region adjacent to the surface is I_{sur} and the leakage current from other possible leakage paths, e.g., corners and measurement noise, is named I_{par}. Since n_i increases due to stress-induced band-gap shrinkage, the diffusion and generation currents in Eq. (4) depend on stress. Fig. 8 shows measured and simulated data for a 1200 diode array with a diode area of 10^{-4} cm^2. The simulated data are with and without TAT. There is good agreement between simulated data (MEDICI), analytic model data (Eq. (4)), and experimental data. The analytic model considers the device stress due to LOCOS and TAT. For simplicity, the stressed intrinsic carrier density is used over the entire junction in the analytic model.

In summary, the perimeter edge areas formed by LOCOS can experience high stress, that can create physical defects, electrical traps, and also higher electric fields due to the physical geometry. These factors are strongly correlated to the leakage current leading to increased current.

4. Gate leakage currents

Leakage currents through dielectrics are considered a major reliability issue in NVMs. As gate oxides become thinner, the conductance of oxide layers increases. For thick oxides ($\geqslant 10$ nm), FN current contributes the major leakage component and direct tunneling current does the same for thin oxides ($\leqslant 3$–4 nm) [12]. An additional oxide leakage current, stress-induced leakage current (SILC) can be generated during device operation. SILC is believed to be due to inelastic tunneling through traps introduced into the oxide by the applied voltage or current [12,13]. SILC is also known to be a major contributor to data retention problems in NVMs. In NVMs, the traps leading to the "disturb" are created by hot carriers during "write" and "erase" cycles, although the exact origins of trap generation are not well understood [14,15].

We used devices with 8 nm thick gate oxide since it is used as the tunnel oxide for the floating gate of memory cells. It is an intermediate thickness oxide between direct tunneling and FN tunneling. We carefully measured and observed a detectable amount of gate leakage current (>10 fA), different from SILC and not transient current, in the low electric field regime as well as FN tunnel currents at high electric fields. We propose a low electric field current component caused by field ionization (FI) tunneling via traps as another possible gate leakage current component, which can lead to "write disturbs". The FI current has a different electric field relationship than SILC and optical excitation increases the FI current, as discussed below.

4.1. The gate leakage current components

Assuming that the normal energy band structure can be applied to an amorphous material, six possible leakage mechanisms are possible in thin insulating films [16]: ionic conduction, space-charge-limited flow, tunneling, Schottky emission, Frenkel–Poole emission, and impurity conduction. In addition, SILC can be observed at moderate electric fields. We propose FI current as an additional current component at low electric fields as shown in Fig. 9. The oxide has been electrically stressed intentionally for the traps to be generated.

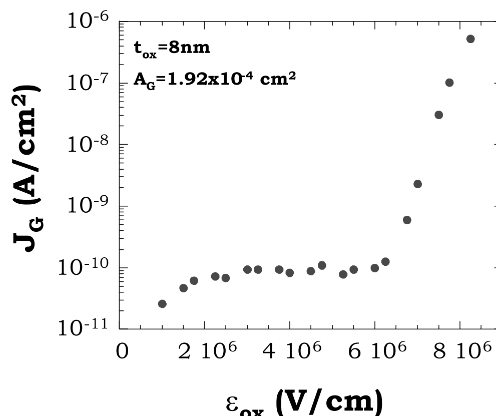

Fig. 9. Gate leakage current through trap-generated oxide. FN tunneling current in the high electric field regime (> 6×10^6 V/cm) and an enhanced current at lower electric fields.

4.2. Field ionization current

The tunnel currents through an oxide are illustrated with the band diagrams in Fig. 10 for an n^+ poly-Si gate and an n-type substrate. Fig. 10(a) shows FN tunneling from the substrate conduction and valence bands for positive gate voltages. Fig. 10(b) shows direct tunneling from the substrate conduction and valence bands. With sufficiently high gate voltages, electrons from conduction and valence bands can tunnel through the oxide as FN or direct tunneling. Although for thin oxides, the primary mechanism is tunneling of electrons from the conduction band, gate leakage current due to tunneled electrons from the valence band is also possible [17]. The FN current is given by

$$I_{FN} = A_G A \varepsilon_{ox}^2 \exp[-B/\varepsilon_{ox}] \tag{5}$$

where A and B are constants [18]. Due to the higher barrier for tunneling from the valence band, both FN and direct tunneling are usually due to electron tunneling from the conduction band.

FI tunneling is illustrated in Fig. 11(a). Electrons tunnel from the substrate into the oxide, where they are trapped and subsequently field ionized into the oxide conduction band. SILC is based on tunneling into the gate via traps, illustrated in Fig. 11(b). Electrons tunnel from the traps or the conduction band to the gate via direct tunneling. An analytic model for SILC was developed based on sequential direct tunneling with 1.5 eV energy loss due to the Jahn–Teller effect [15]. This analytic model for SILC is based on the Esaki–Tsu equation [19]. Electrons tunnel through the triangular energy barrier to the gate during FI. Its tunneling probability can be calculated with the WKB approximation. With the gate under constant voltage or constant current stress, traps can be generated within the oxide. The traps are mainly distributed $2 \sim 3$ eV below the oxide conduction band [20]. We stressed the gate oxide, which has the area of 8.5×10^{-8} cm^2 with positive gate voltage at a current of 10 nA for a fluence of 1 C/cm^2. There are distinct differences for the oxides before and after stress. The current increase is related to the trap generation within the oxide. Initially the unstressed oxide allowed only FN tunnel current but oxides stressed at low leakage currents showed an additional FI current component in the low electric field regime as shown in Fig. 12.

The tunneling transition tunnel probability through a triangular barrier is given as

$$f = \exp\left(-\frac{4\sqrt{2m^*}}{3qh}\frac{E_I^{3/2}}{\varepsilon_{ox}}\right) \tag{6}$$

where E_I is the ionization energy and ε_{ox} the oxide electric field. The FI current can be expressed as [21]

$$I_{FI} = A_G C \varepsilon_{ox} \exp\left(-\frac{4\sqrt{2m^*}}{3qh}\frac{E_I^{3/2}}{\varepsilon_{ox}}\right) = A_G C \varepsilon_{ox} \exp\left(-\frac{D}{\varepsilon_{ox}}\right) \tag{7}$$

where A_G is the gate area, and C and D are constants. The electric field across the oxide can be written as

$$\varepsilon_{ox} = \frac{(V_G - V_{FB} - \phi_s - \phi_{gate})}{t_{ox}} \approx \frac{V_G}{t_{ox}} \tag{8}$$

where V_{FB} is the flatband voltage, ϕ_s the substrate surface potential and ϕ_{gate} the gate surface potential.

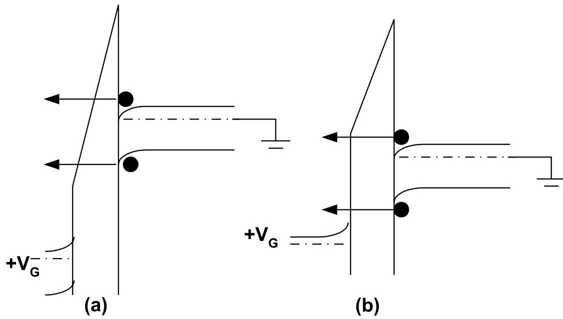

Fig. 10. (a) Fowler–Nordheim tunneling (b) direct tunneling.

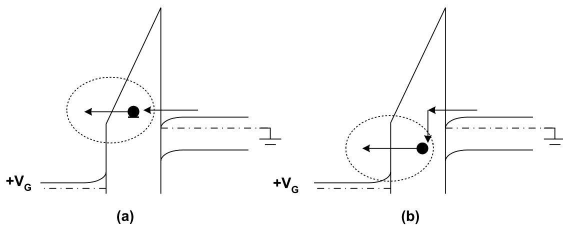

Fig. 11. (a) Field ionization (b) stress-induced leakage current mechanisms.

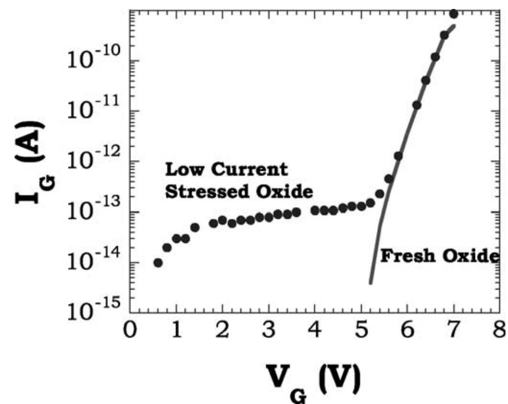

Fig. 12. The gate currents through fresh and stressed oxide.

Assuming negligible oxide charges, $V_{FB} = -(kT/q)\ln(N_{gate}/N_{sub}) \approx -0.24$ V for n$^+$ poly-Si gates and n-type substrates ($N_D = 6 \times 10^{16}$ cm^{-3}). Also we accumulate the substrate surface using positive gate voltage and ignore ϕ_s, ϕ_{gate} and V_{FB} for high gate voltages. Eq. (7) can be rewritten as

$$\ln\left(\frac{I_{FI}}{V_G}\right) = \ln\left(\frac{A_G C}{t_{ox}}\right) - \frac{Dt_{ox}}{V_G} \quad (9)$$

A plot of $\ln(I_{FI}/V_G)$ vs. $1/V_G$ has a slope of $-Dt_{ox}$ and intercept of $\ln(A_G C/t_{ox})$. Writing the FN expression, Eq. (5), in the form of Eq. (9) gives the slope $-Bt_{ox}$. The coefficient B and D are given by

$$B = \frac{4\sqrt{2m^*}(q\Phi_B)^{3/2}}{3q\hbar}; \quad D = \frac{4\sqrt{2m^*}E_I^{3/2}}{3q\hbar} \quad (10)$$

where $q\Phi_B$ is the barrier height at the SiO_2/Si interface. Since $q\Phi_B$ is typically higher than E_I, we find the slope of FN-dominated gate current plot to be steeper than that due to FI current. The slopes are commonly used to determine $q\Phi_B$ and E_I.

For a better understanding of the gate leakage current mechanism, we measured the gate leakage current at different temperatures over the $T = 300$ to 473 K range. It is insensitive to temperature as shown in Fig. 13 showing that tunneling is the main mechanism. It also shows that Schottky and Frenkel–Poole emission currents can be ruled out since they are strongly temperature dependent.

Fowler–Nordheim current is significant at high electric fields. SILC is observed at lower electric fields and is less electric field dependent than FN current. FI is still less electric field dependent. The slopes of each current, illustrated in Fig. 14, indicate the electric field sensitiveness for each mechanism.

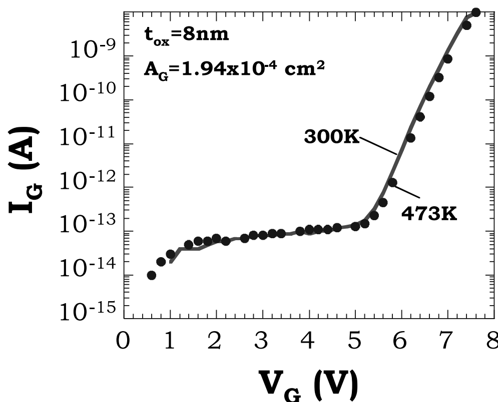

Fig. 13. Gate leakage current at different temperatures.

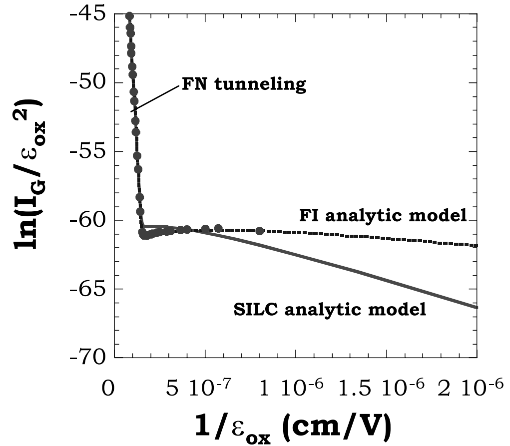

Fig. 14. Fowler–Nordheim plots for FN, SILC and FI currents. Points: experimental data; lines: theory.

4.3. Photo-ionization and Franz–Keldysh effect

Previously we assumed the majority of oxide traps to be distributed as deep-level traps. If that is a valid assumption, then it should be possible to observe photo-ionization. Theoretical and experimental photo-ionization from deep-level traps is well known in optoelectronics [22,23]. In 1958 Franz and Keldysh independently proposed photon-assisted tunneling. Trapped electrons in SiO_2 "see" the energy barrier E_I, shown in Fig. 15. When the sample is illuminated, photons, absorbed by the trapped electron, raise the electron energy thereby reducing the barrier to $E_I - E_{opt}$. This reduces not only the energy barrier but also the tunnel distance, leading to excess current.

In order to reduce absorption within the n$^+$ poly-Si gate we used a red-light emitting diode (LED), $\lambda = 660$ nm with a penetration depth of approximately 3 μm in Si. Since positive gate voltage brings the n-type substrate into accumulation and the optically generated electrons within the semiconductor are sufficiently low to be ignored, the Franz–Keldysh effect only takes place within

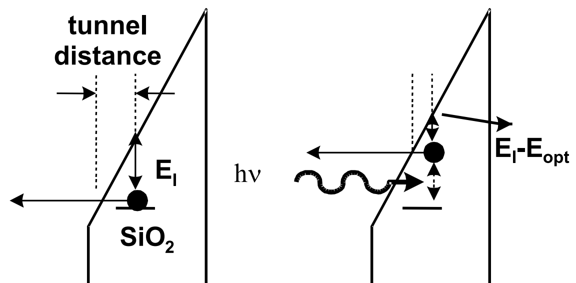

Fig. 15. The reduction of tunneling barrier and distance with photon absorption.

the oxide. We used two different gate oxides, one was a fresh, unstressed oxide and the other was a trap generated, stressed oxide. For the fresh oxide, we measured no significant change of oxide leakage current with and without light indicating that few deep-level oxide traps existed and FN tunneling current is the dominant current mechanism as shown in Fig. 16.

However, for the oxide containing traps, we observed significant gate oxide leakage currents between illumination and no illumination shown in Fig. 17. Without LED illumination, the current is caused by field ionization. The optical excitation increases the current further.

The leakage current through the stressed oxide with the Franz–Keldysh effect can be expressed as

$$I_G = I_{FI} + I_{opt} + I_{FN} \approx I_{opt} + I_{FN} \tag{11}$$

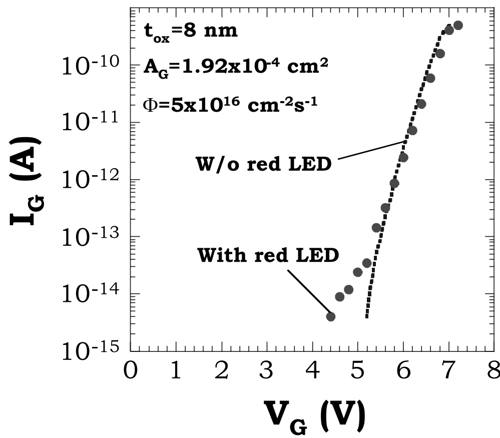

Fig. 16. Gate current through an unstressed oxide with and without LED illumination.

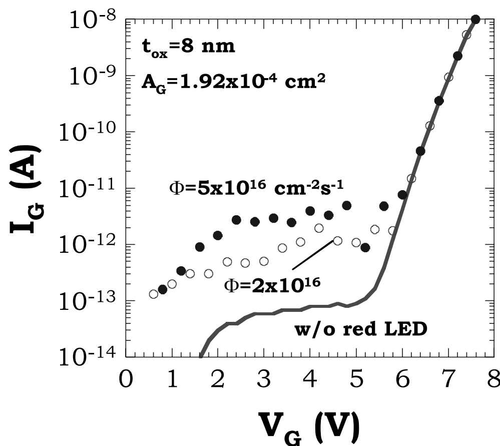

Fig. 17. Optically generated gate current due to the Franz–Keldysh effect.

$$I_{opt} = qA_G(1-R)\Phi(1-\exp(-\alpha_{FK}t_{ox})) \approx qA_G(1-R)\Phi\alpha_{FK}t_{ox} \tag{12}$$

for $\alpha_{FK}t_{ox} \ll 1$, where Φ is the photon flux density, R the reflectivity, and α_{FK} the optical absorption coefficient. The absorption coefficient is given by

$$\alpha_{FK} = \frac{A''E_{ox}}{E_I - \hbar\omega}\exp\left(-\frac{B''(E_I-\hbar\omega)^{3/2}}{E_{ox}}\right) \tag{13}$$

Since the current due to the Franz–Keldysh effect is due to electron tunneling through the triangular barrier, similar to the field ionization tunneling current, as shown in Fig. 17, the current and electric field relationships are very similar and I_{opt} and I_{FI} can be expressed as

$$I_{opt} = qA_G(1-R)\Phi\alpha_{FK}t_{ox} = A1''E_{ox}\exp\left(-\frac{B1''}{E_{ox}}\right) \tag{14}$$

$$I_{FI} = A_GBE_{ox}\exp\left[-\frac{4\sqrt{2m^*}}{3\hbar q}\frac{E_I^{3/2}}{E_{ox}}\right] = A_GBE_{ox}\exp\left[-\frac{C}{E_{ox}}\right] \tag{15}$$

To determine the stress-generated trap density, we determined the voltage shift with capacitance–voltage measurements of MOS capacitors before and after stress. A voltage shift of 0.2 V resulted from a trap density of $N_t \approx 10^{17}$ cm^{-3}. The gate leakage current for the Franz–Keldysh effect is proportional to the absorption coefficient, α_{FK}. Hence α_{FK} can be extracted from the low electric field current

$$\alpha_{FK} = \frac{I_{opt}}{qA_G(1-R)\Phi t_{ox}} = N_t\sigma_{opt} = 0.03\ \text{cm}^{-1} \tag{16}$$

This gives $\sigma_{opt} \approx 3\times10^{-19}$ cm^2, similar to the optical capture cross-section of neutral traps, 10^{-18} cm^2, studied

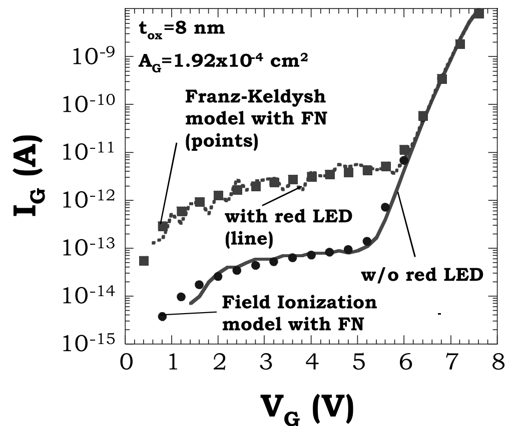

Fig. 18. Measured and modeled I_G–V_G curves.

by Ielmini et al. [24]. Finally, we compared the analytic models for SILC and FI to the experimental data. Although the differences between SILC and FI are small, the experimental data provide better agreement with the FI model than with SILC. The FI current is less sensitive to gate electric field, as shown in Fig. 18.

5. Summary

Floating-gate-based NVMs utilize threshold voltage shifts so it is crucial to retain charges in floating gates without undesired *disturbs*. Two major leakage current components causing disturbs are illustrated in the half cross-section of a NVM cell in Fig. 19. High junction leakage currents can be generated in the pn junction under high reverse bias conditions during "write" and "erase". Unintentional charge injection into floating gates can be due to the junction leakage current and the gate leakage current that is proportional to the junction leakage current. Low leakage current through the floating gate also occurs at low electric fields. The leakage current depends on the gate oxide integrity and stress as shown in Fig. 16. Stressed oxide allows more gate leakage current into the floating gate than a fresh oxide under low electric fields although the FN tunnel current becomes dominant at high electric fields for both cases. We found the low leakage current to be caused by FI from traps within the gate oxides. Although the gate leakage current is low, it can lead to sufficient charge accumulation to disturb charge in the floating gate.

As NVMs are scaled down, electric fields tend to increase. These high fields can degrade the oxide integrity by introducing charges inside the oxide and inject charges into the floating gate. Another type of disturb can also be caused by trapped charges within the oxide. After several repetitions of "write" and "erase", charges may be trapped in the oxide and cause unintentional threshold voltage shift although this does not charge or discharge the floating gate.

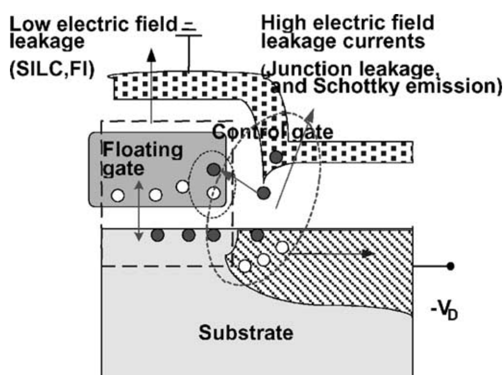

Fig. 19. Leakage currents in a floating-gate-based NVM.

Through detailed simulations and measurements, we have determined the main cause of "write disturb" and "erase disturb" to be field ionization gate oxide current at low electric fields and Fowler–Nordheim current at high electric fields. Additional factors are high-energy electrons from the junction leakage current. A solution to this problem is to reduce the junction leakage current through junction process design to minimize stress and to grow oxides with minimal trap densities.

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