

Impact of channel carrier displacement and barrier height lowering on the low-frequency noise characteristics of surface-channel n-MOSFETs

A.K.M. Ahsan *, D.K. Schroder

Department of Electrical Engineering and Center for Low Power Electronics, Arizona State University, Tempe, AZ 85287-5706, USA

Received 27 August 2004; received in revised form 13 December 2004; accepted 1 January 2005

The review of this paper was arranged by Prof. S. Cristoloveanu

Abstract

Several unified low-frequency noise models for MOSFETs, developed in the past, combine carrier number fluctuations and correlated mobility fluctuations. The characteristics of the physical parameters in these models are reevaluated here, considering the channel carrier density and their displacement from the oxide–semiconductor interface with applied gate and body bias. The lowering of the oxide–semiconductor tunneling barrier with increasing gate bias is also considered for noise calculations. Experimental results are reported for n-MOSFETs to compare with the calculated low-frequency noise considering these effects. Including the oxide–semiconductor barrier height lowering and average displacement of channel carriers in the conventional correlated low-frequency noise model, the bias and geometry dependence of $1/f$ noise is explained quantitatively.

© 2005 Elsevier Ltd. All rights reserved.

Keywords: Low-frequency noise; Oxide trap density; Scattering parameter; Barrier height lowering; Quantum effects; Correlated noise model; Silicon; MOSFET

1. Introduction

Theoretical and experimental studies on MOSFET noise have revealed the different types of noise and their characteristics for both long- and short-channel MOSFETs. Thermal noise, shot noise, generation-recombination noise, and low-frequency noise are the dominant noises. Low-frequency noise is prominent in MOSFETs due to the heterogeneous interface between silicon and silicon dioxide. Since the early days of low-frequency noise research in MOSFETs, it has been exhaustively

demonstrated that the low-frequency or $1/f$ noise dominates in the lower part of the frequency spectrum ($f < 10$ kHz). This type of noise is characterized by a power spectrum density, which varies according to a $1/f^\gamma$ law with $\gamma = 0.7$ – 1.2 . Originally it was thought that $1/f$ noise in semiconductor devices is a surface phenomenon and, therefore, is directly related to the quality of the Si–SiO₂ interface. Different models are proposed which fall roughly under two categories. One is the number fluctuation or ΔN theory [1–4] and the other is the mobility fluctuations $\Delta\mu$ theory [5–7]. It has also been suggested that lattice scattering causes $1/f$ noise [8,9]. Some models explain the correlated nature of carrier number and mobility fluctuations [10–12]. According to correlated theory, near-interface traps, also known as border traps [13–15], are responsible for trapping

* Corresponding author. Address: Solid-State Device, INTEL Corporation, 20459 NW, Anzalone Dr, APT253, Aloha, OR 97006, United States. Tel.: +1 2145298748; fax: +1 9712149185.

E-mail address: akm.a.ahsan@intel.com (A.K.M. Ahsan).

and detrapping of the channel carriers. The trapped charge then plays the role of a Coulombic site leading to Coulombic scattering of trapped charge so that number and mobility of channel carriers fluctuate with time. A comparative discussion on number and mobility fluctuation is presented in the next section.

2. Theoretical background of $1/f$ noise

Several theories have been presented to explain the origin of $1/f$ noise. In one approach, the $1/f$ noise is explained successfully by carrier-number fluctuations ΔN , which are caused by tunneling of free-charge carriers into oxide traps close to the Si–SiO₂ interface. The observed proportionality between trap density and $1/f$ noise support the ΔN concept. The other school of thought considers $1/f$ noise a bulk phenomenon due to mobility fluctuation. This school of thought uses an empirical relation where the relative $1/f$ noise is inversely proportional to the number of carriers and proportional to a dimensionless parameter α_H . For n or p-type Si bulk samples at $T = 77$ K or at 300 K the value of α is about 2×10^{-6} (for impurity concentrations lower than 10^{16} cm^{-3}) [16]. For impurity concentration of 10^{17} cm^{-3} , the carrier mobility and also the α value are reduced. The gate voltage noise spectrum density for MOSFETs in the ohmic region can be expressed by the equation [17]

$$S_{vG} = \frac{\alpha_H q (V_G - V_T)}{WLC_{ox}f} \quad (1)$$

where C_{ox} is the oxide capacitance, WL is the gate area and the gate overdrive voltage is taken as positive for p-MOSFETs.

The surface origin of $1/f$ noise is described on the basis of the McWhorter number fluctuation theory [1]. The evidence of the change in $1/f$ noise through degradation by hot electrons [18–20] or by ionizing irradiation [21–23] support the number fluctuation theory. It was also observed experimentally that $1/f$ noise in n-MOSFETs can be well explained by the popular ΔN theory [2,3,11,12], where as the explanations are not robust for p-MOSFETs. p-MOSFETs are less noisy and the $1/f$ noise for this type of devices is often easier to interpret in terms of the $\Delta\mu$ theory than in terms of the ΔN theory [24–27].

After much controversy, the unified correlated model was proposed by Hung et al. [10,11] where both the number and mobility fluctuations were taken into account in a correlated fashion. This model explains $1/f$ noise of n-MOSFETs successfully. According to this model, the drain current noise spectrum density and the gate voltage noise spectrum density for MOSFETs in the strong inversion and linear region can be expressed by

$$S_{ID}(f) = \frac{kT\mu_D^2}{\alpha W L f} \left(\frac{1}{N_s} + S\mu_{\text{eff}} \right)^2 N_{\text{ot}}(E_{\text{Fn}}) \quad (2)$$

$$S_{vG}(f) = \frac{kTq^2}{\alpha W L C_{ox}^2 f} (1 + S\mu_{\text{eff}} N_s)^2 N_{\text{ot}}(E_{\text{Fn}}) \quad (3)$$

where W is the gate width; L , the gate length; μ_{eff} , the effective carrier mobility; N_s , the number of channel carriers per unit area; S , the scattering parameter; α , the attenuation constant; C_{ox} , the oxide capacitance; $N_{\text{ot}}(E_{\text{Fn}})$ the oxide trap density at the quasi-Fermi level, and f is the frequency. For MOSFET operation in the saturation region, the carrier density along the channel is not uniform and the above expressions need to be modified. Eq. (2) reveals that $1/f$ noise is generated by both number and mobility fluctuations. Number fluctuation is proportional to $1/N_s$ and the mobility fluctuation is proportional to $S\mu_{\text{eff}}$. From Eq. (3) we understand that at low gate voltages, the correlated model reduces to the conventional number fluctuation model since N_s is very low in weak inversion. It reveals the fact that number fluctuation dominates when the carrier density is low. To calculate the noise power spectrum density, the values and characteristics of the scattering parameter S , the attenuation coefficient α , and the oxide trap density $N_{\text{ot}}(E_{\text{Fn}})$ need to be known for different bias conditions. For most cases, α is calculated theoretically, whereas S is determined both theoretically and experimentally.

In the basic unified model, the scattering parameter is introduced to define the scattering strength of the channel carriers by the near-interfacial oxide charges. This parameter has been calculated theoretically [28–31] and was also determined experimentally by using the measured mobility limited by Coulombic scattering [11,29,32]. The scattering parameter is bias dependent and only the carrier screening effect is considered to explain the bias dependence ignoring the channel carrier displacement from interface. The channel carrier location below the SiO₂/Si interface with applied bias also affects the Coulombic scattering rate of carriers by trapped oxide charges. The other important parameter to calculate $1/f$ noise is the attenuation constant [3], which is typically expressed as

$$\alpha = \sqrt{\frac{2m_e^* \phi_{ox}}{\hbar^2}} \quad (4)$$

where m_e^* is the oxide effective electron mass and ϕ_{ox} the oxide–semiconductor barrier height. This attenuation constant depends on the oxide–semiconductor energy barrier because carriers tunnel into the oxide through the energy barrier ϕ_{ox} . α is usually considered constant and its value is typically taken to be 10^8 cm^{-1} using the WKB approximation. However, to determine the value of α precisely, barrier height lowering of the

oxide–semiconductor energy barrier by the oxide electric field must be taken into account.

In this paper, we consider the bias dependence of the scattering parameter of channel carriers in terms of both carrier screening [33] and carrier displacement from the SiO₂/Si interface with applied gate and body bias. We also consider barrier height lowering with applied gate voltage to calculate the attenuation constant accurately. We assumed that the near-interfacial trap charge density does not change with gate voltage as it was proposed and proved in Scofield et al. paper [26]. In that work, they support with appropriate validation that $1/f$ noise of both n and p-MOSFET is due to trapping–de-trapping mechanism, with trap density nearly constant for n-MOS transistors and varying with gate voltage for p-MOS transistors. The present work is solely based upon the performance of n-MOSFET where the trap density tends to be weakly dependent on the trap energy in the range of E typically accessed with room temperature operation. Experimental results for gate and body bias dependence are reported to validate our theory. The experimental observation of body bias dependence of low-frequency noise is also explained quantitatively.

3. Scattering parameter and attenuation constant

3.1. Scattering parameter

The scattering parameter in the unified model represents the strength of Coulombic scattering of channel carriers by oxide trap charges that affect the carrier mobility. Using Mathiessen's rule, the effective carrier mobility can be expressed by [11]

$$\frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_n} + SN_t \quad (5)$$

where μ_n is the effective mobility limited by all the scattering mechanisms except Coulombic scattering by oxide charges; S , the scattering parameter in V -s, and N_t is the occupied trap density per unit area. Theoretical and experimental studies have shown that the scattering parameter is not constant but depends on the degree of inversion due to carrier screening. When a charge is placed in an electron gas, mobile electrons adjust to cancel the charge and the net result is a screened potential, which alters the Coulomb potential of the point charge. Channel carriers are screened at high vertical electric fields. Raising the gate voltage increases the number of inversion carriers, reducing the scattering rate of the carriers by the Coulombic influence of surface oxide charges. Analysis and measurement [32,34,35] explain the bias dependence of the scattering parameter due to carrier screening.

Here we introduce the concept that this parameter is also a function of the average distance of the carriers

from the interface. Classical and quantum analysis of the inversion carriers shows that the average distance of the carriers from the SiO₂/Si interface increases as the degree of inversion is reduced from strong inversion to weak inversion. In Fig. 1 we compare the quantum and classical distribution of channel carriers in a MOSFET at two different gate voltages. It is obvious that the inversion layer charge should not be considered as a sheet charge; rather it has a finite thickness. The average distance of carriers is the distance of the carrier centroid from the interface that can be expressed by

$$x_{\text{avg}} = \frac{\int_{x_a}^{x_b} x N_s dx}{\int_{x_a}^{x_b} N_s dx} \quad (6)$$

where x_a is the surface and x_b the bulk (the neutral region under the depletion region). N_s is the inversion carrier density, which is a function of distance from the interface into the bulk silicon. In Fig. 2 we plot

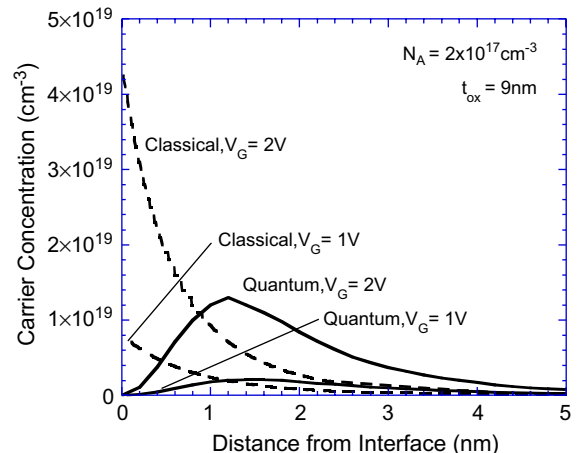


Fig. 1. Channel carrier distribution versus distance from the SiO₂/Si interface for classical and quantum calculations at two different gate voltages.

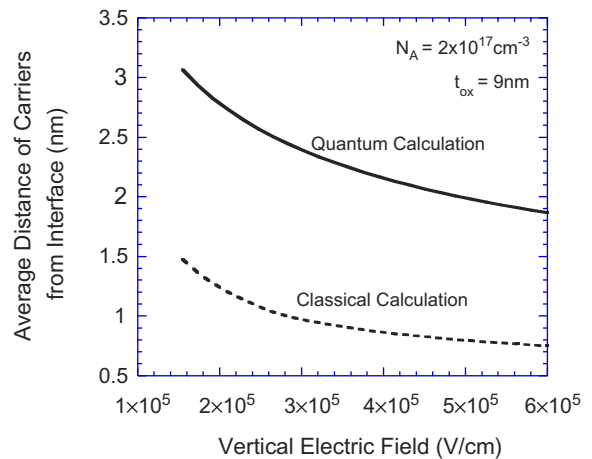


Fig. 2. Average distance of channel carriers from the SiO₂/Si interface versus vertical electric field.

the average distance of channel carriers versus the gate voltage in a typical MOSFET. These simulation results have been generated from the full solution of the silicon inversion layer in MOSFET, obtained by numerically solving the coupled Poisson's and Schrödinger's equations self-consistently [36,37]. The oxide thickness and channel doping concentration in these simulation were 9 nm and $2 \times 10^{17} \text{ cm}^{-3}$.

It has been reported [29] that the Coulombic scattering limited mobility of the oxide trapped charges, μ_c , is proportional to the square root of the inversion carrier density, N_s and can be represented by

$$\mu_c = \mu_{co} \frac{\sqrt{N_s}}{N_t} \quad (7)$$

where μ_c is the mobility limited by Coulombic scattering in cm^2/Vs , $\mu_{co} = 5.9 \times 10^8 \text{ cm}^2/\text{Vs}$; N_s , the inversion carrier density in cm^{-2} , and N_t is the near-interfacial oxide trap charge density in cm^{-2} . The value of μ_{co} has been extracted from the experimental results on Coulombic scattering limited mobility, obtained from improved split capacitance–voltage measurements. Using Eqs. (7) and (5) we get an expression of the bias dependent scattering parameter $S(V_G)$, which agrees with the experimental results, given by

$$S(V_G) = \frac{1}{\mu_{co} \sqrt{N_s}} \quad (8)$$

Eq. (8) predicts the dependence of the scattering parameter on the degree of inversion due to the screening effect and this variation is plotted in Fig. 3. The scattering cross section of the screened Coulombic scattering has been calculated by Soppa and Wagemann [31]. Nicollian and Brews [38] calculated the screening length and found that it is inversely proportional to the sum of oxide capacitance, inversion capacitance, depletion region capacitance and interface state capacitance. For a high degree of inversion, the screening length reduces

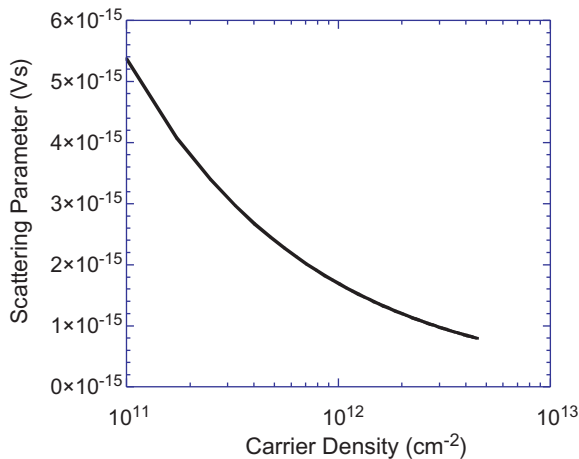


Fig. 3. Scattering parameter versus channel carrier density. Only carrier screening is considered.

leading to a smaller scattering coefficient. As a result, the strength of Coulombic scattering reduces, represented by a reduced value of the scattering parameter.

It is obvious that the scattering rate is a bias-dependent parameter and it varies significantly with applied bias due to carrier screening. Additionally, we propose that the scattering parameter also depends on the distance of the inversion carriers from the interface. From the work done by Brews [28,38], we know that the Coulombic scattering potential decreases as the distance between the source charge and the scattered charge increases. Influence of near-oxide interfacial charge on the inversion layer mobility has been discussed in [39]. Following similar type of approach and based on the Brews work [28] on Coulombic scattering-limited mobility, we assume the following approximate dependence of scattering parameter on the location of inversion charge from the interface

$$S(V_G, x_d) = S_{\text{avg}}(V_G) \ln \left[1 + \left(\frac{r_{\text{max}}}{x_d} \right)^2 \right] \quad (9)$$

where $S_{\text{avg}}(V_G)$ is the average scattering parameter, that depends on the applied bias due to carrier screening. It represents the weighted average of various scattering parameters corresponding to different oxide charges located at various distances into the oxide from the interface. x_d is the average displacement of carriers from the interface, defined as $x_d = x_{\text{avg}}(V_G) - x_{\text{avg0}}$, where $x_{\text{avg}}(V_G)$ is the average distance of the carriers from the interface at a gate voltage above threshold, x_{avg0} is the average distance of carriers at the onset of inversion, and r_{max} is the maximum distance from the scattering charge for which the image charges can be neglected. Actually, oxide trap charges are distributed at various distances into the oxide from the interface and each trapped charge contributes to the Coulombic scattering of the inversion carriers. Hence, the values of scattering parameter shown in Fig. 3 are the average of all scattering components.

In Fig. 4 we have plotted the scattering parameter with vertical electric field ignoring carrier screening and considering carrier displacement only. To observe the variation of S with vertical electric field (with the average distance of carriers from interface) without considering the screening effect, we have assumed $S_{\text{avg}}(V_G)$ to be constant and the appropriate value is taken from the data presented in Fig. 3. To calculate $1/f$ noise using the correlated model, we consider both effects to determine the value of the scattering parameter as a function of applied bias.

3.2. Attenuation constant

The Si–SiO₂ energy barrier ϕ_{ox} is defined as the energy difference between the SiO₂ and the Si conduction

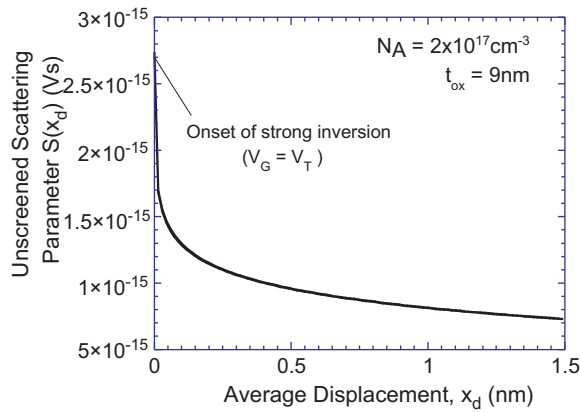


Fig. 4. Unscreened scattering parameter versus average displacement of inversion carriers from the SiO₂/Si interface with applied gate bias.

bands. However, as the electrons are emitted from Si into SiO₂, the actual energy barrier to emission is reduced by the Schottky barrier lowering effect. Schottky barrier lowering is expressed as

$$\Delta\phi = \sqrt{\frac{q^3 E_{\text{ox}}}{4\pi\epsilon_{\text{ox}}}} \text{ (eV)} \quad (10)$$

where E_{ox} is the oxide electric field. The effective energy barrier to emission is then $\phi_{\text{ox}} - \Delta\phi$. The carriers in the MOSFET channel tunnel into the oxide traps and their random trapping and detrapping causes low-frequency noise.

The attenuation constant has a typical value of 10^8 cm^{-1} . However, to determine its value precisely, image force barrier-lowering [40] of the oxide–semiconductor energy barrier needs to be taken into account. Eq. (10) shows that the oxide–semiconductor barrier is not a constant but depends on the oxide electric field, i.e., the applied gate voltage and α can be expressed by

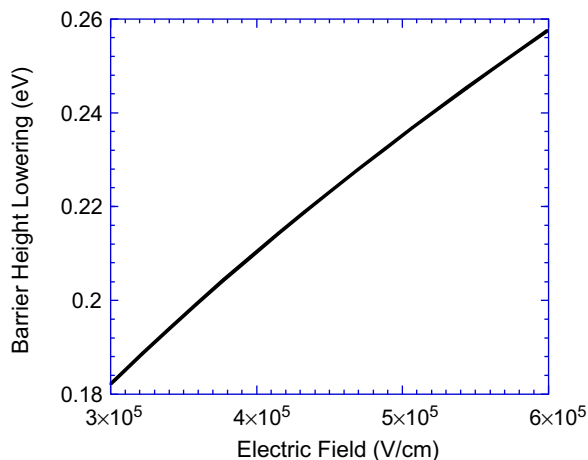


Fig. 5. Barrier height lowering versus vertical electric field.

$$\alpha(V_G) = \sqrt{\frac{2m_c^*(\phi_{\text{ox}} - \Delta\phi(V_G))}{\hbar^2}} \quad (11)$$

We have calculated the oxide–semiconductor barrier height for tunneling of electrons into the oxide traps for different gate voltages. The change in the barrier height with vertical electric field is plotted in Fig. 5. The exact value of α with bias is obtained from Eq. (11) and it is used in the unified model to determine the drain current and gate voltage noise spectrum densities.

4. Experimental results and discussion

The test devices (n-MOSFETs) were fabricated in a 0.35 μm CMOS technology with a threshold voltage $V_T = 0.6 \text{ V}$. The thermally grown gate and field oxide thicknesses are 9 nm and 620 nm respectively. Source/drain junction depths are 0.25 μm . The MOSFETs have a wide range of gate areas, from $1000 \times 4 \mu\text{m}^2$ to $20 \times 0.75 \mu\text{m}^2$. The experimental setup, shown in Fig. 6, allows automated measurement of drain current noise for various gate–source, drain–source and bulk–source voltages. The noise is measured with the BTA 9812A system, consisting of a controller unit and an amplifier/filter unit used for detection and amplification of the noise voltage and current generated by the device under test (DUT). The BTA 9812A also filters out the noise from the bias voltage or current sources applied to the device. A semiconductor parameter analyzer (HP4142B) is used for the generation of DC biases for the DUT and for measurement of the device I – V characteristics: threshold voltage (V_T), drain to source current (I_D), transconductance (g_m) and drain to source conductance (g_d). These measured parameters are used to calculate the drain current noise spectrum density (S_{ID}) and input referred noise spectral density (S_{VG}), as well as for modeling purpose.

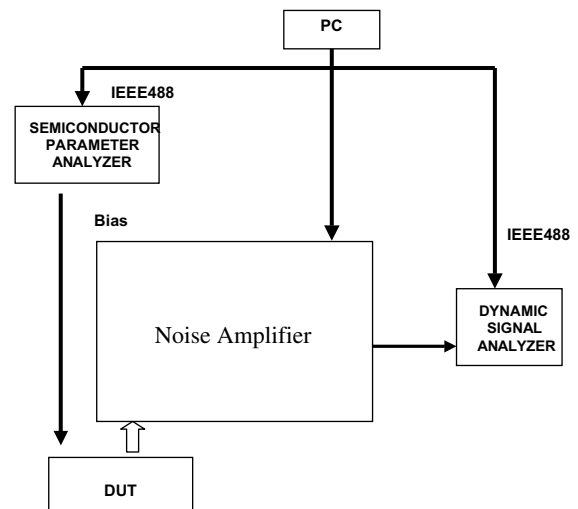


Fig. 6. Experimental setup for automated noise measurement.

A dynamic signal analyzer (HP35665A) is used to measure the low-frequency noise spectrum density from 1 Hz to 10⁶ Hz. The digital signal analyzer can store several traces in time or frequency and perform operations such as multiplication or division of stored traces by each other or by constants. Another feature allows averaging, which combines newly measured data with previously measured data on a point-by-point basis using a root mean square calculation. This averaging feature is very useful to minimize the fluctuation in data, which increases for smaller devices. A PC controls the equipment through an IEEE-488 (GPIB) bus. The NoisePro for windows software controls the equipment for automatic noise and *I-V* measurements. The program can also process the measured data and extract all the required model parameters for simulation of noise characteristics of a single device or the entire circuit.

Several physical parameters for low-frequency noise modeling were extracted from the measured *I-V* characteristics. The threshold voltage, drain current in the linear and saturation regions, transconductance, drain conductance, effective mobility, channel carrier concentration, etc. were extracted from the experimental *I-V* plots. The experimental *I_D-V_G* characteristics and extracted carrier density are plotted in Fig. 7(a) and (b), respectively. The drain voltage was kept at 0.1 V with no body bias. The effective mobility is extracted from the measured *I-V* characteristics.

The drain current noise spectrum densities for *f* = 100 Hz are plotted against gate overdrive voltages at *V_{DS}* = 1.2 V in the strong inversion region in Fig. 8. Both of the simulation results considering and without considering channel carrier displacement and barrier height-lowering with applied gate bias are compared with the experimental values. The corrected simulation results using the modified approach in determining the scattering parameter and attenuation constant showed excellent agreement with the measured results. On the other hand, the simulation result assuming constant attenuation constant with applied bias and decreasing scattering parameter due to only carrier screening affect

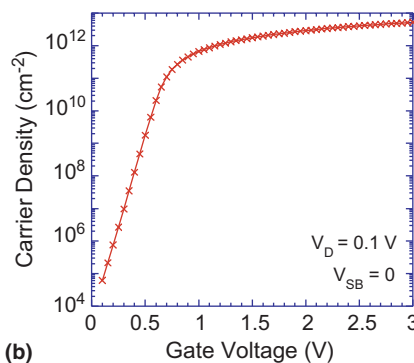
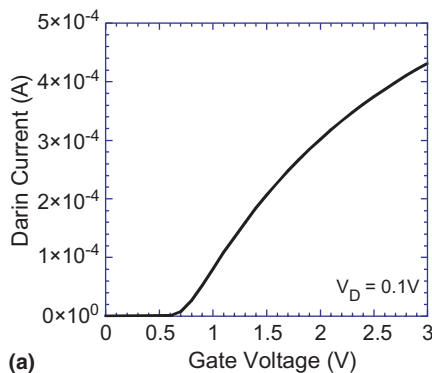


Fig. 7. (a) *I-V* characteristics of n-MOSFET with *W/L* = 20/1 and *t_{ox}* = 9 nm, (b) extracted channel carrier density from experimental *I-V* plot.

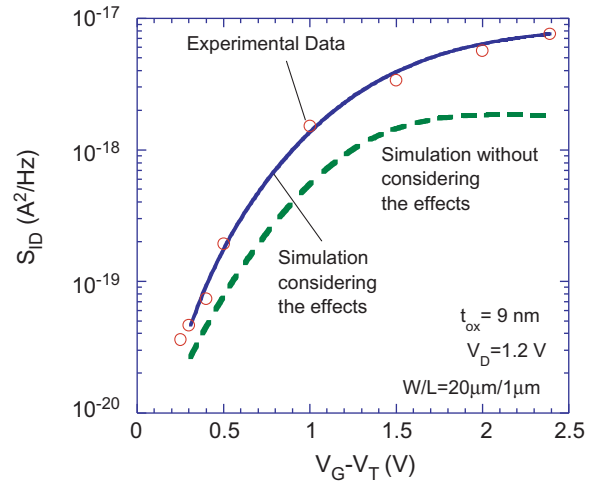


Fig. 8. Drain current noise spectrum density versus gate overdrive voltage at high drain voltage at *f* = 100 Hz. Simulation and measured results are represented by solid and dotted lines and points, respectively.

deviates by more than half an order of magnitude from the measured results at high gate overdrive voltages. It is obvious from the two simulated plots that at relatively low gate overdrive voltage (less than 0.5 V) channel carrier displacement and barrier-height lowering effect are negligible, whereas, at higher gate overdrive voltage carriers come closer to interface and barrier height lowering is significant and the conventional correlated model underpredicts the noise in this region. The simulated results are shown in the saturation region of operation. At high drain voltage, the carrier density and mobility are nonuniform along the channel. In general, the effective mobility of the carriers depends on the horizontal electric field according to Eq. (12) and particularly at high drain voltage this dependence becomes significant.

$$\mu'_{\text{eff}}(y) = \frac{\mu_{\text{eff}}}{(1 + (E(y)/E_c)^2)^{1/2}} \quad (12)$$

where $\mu'_{\text{eff}}(y)$ is the effective mobility, μ_{eff} is the effective mobility without considering the dependence on

horizontal electric field, $E(y)$ is the electric field along the channel and E_c is the critical electric field at which the carrier velocity saturates. The carrier density N_s depends on the channel potential, which varies with the distance from the source end to the drain end. Thus, the carrier density can be expressed as

$$N_s(y) = \frac{C_{ox}}{q[V_G - V_T - V(y)]} \quad (13)$$

where $V(y)$ is the channel potential at point y measured from the source junction. C_{ox} , V_G and V_T are the oxide capacitance, gate voltage and threshold voltages, respectively. The channel potential $V(y)$ has the analytical expression [42]

$$V(y) = \frac{V_G - V_T}{m} - \sqrt{\left(\frac{V_G - V_T}{m}\right)^2 - 2\frac{y}{L}\left(\frac{V_G - V_T}{m}\right)V_D + \frac{y}{L}V_D^2} \quad (14)$$

where m is the body factor. By using this expression we can calculate $N_s(y)$ and $\mu'_{eff}(y)$ at different drain voltages. Eq. (14) suggests that at very low drain voltage $V(y)$ is so low that the carrier density in the channel is almost uniform from source to drain end and Eq. (13) simplifies to $N_s = C_{ox}/q(V_G - V_T)$ which was used for the typical calculation of noise at low drain voltages. At high drain voltage we have taken Eqs. (12) and (13) into account to calculate the noise spectrum density using Eqs. (2) and (3). The gate voltage noise spectrum densities for various gate areas are plotted against gate overdrive voltages at $V_D = 0.1$ V in the strong inversion region in Fig. 9 at $f = 100$ Hz. The simulation results including

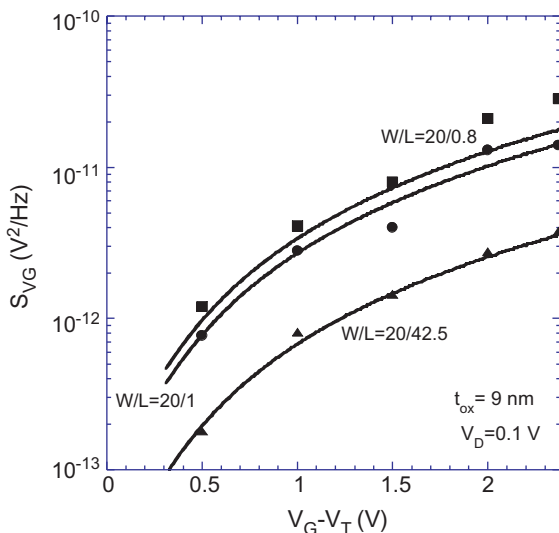


Fig. 9. Gate voltage noise spectrum density versus gate overdrive voltage for different gate areas at $f = 100$ Hz. Simulation and measured results are represented by lines and points, respectively.

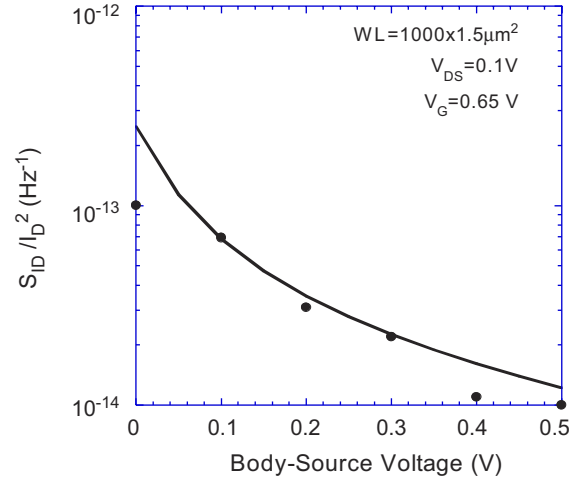


Fig. 10. Normalized drain current noise spectrum density versus forward body bias. Calculated and experimental results are represented by line and points, respectively.

carrier displacement and barrier-height lowering show good agreement with experimental results.

Among the studies for the bias dependence of $1/f$ noise, the body bias dependence of $1/f$ noise is rarely reported. Our experimental results show that $1/f$ noise decreases with forward body bias, specially at low gate voltage. We explain this phenomenon with the modified low-frequency model. The experiments are made on two lots, each containing two wafers, i.e., measurements are made on four wafers from two different lots. The same type of noise behavior from each set of measurements is observed. Fig. 10 shows the normalized noise current spectrum density variation with applied forward body bias at low gate voltage.

For a constant gate voltage, increasing forward body bias reduces the threshold voltage, as a result the number of carriers in the channel increases. Moreover, the scattering parameter decreases due to the carrier

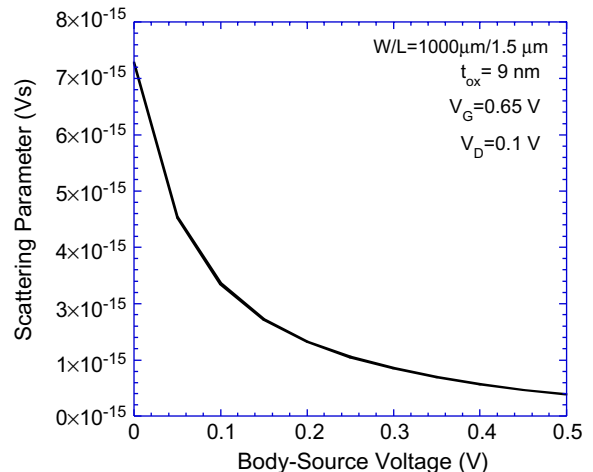


Fig. 11. Scattering parameter versus forward body bias.

screening effect as the number of inversion carrier increases with forward body bias. In Fig. 11, the scattering parameter is plotted against forward body bias.

According to Eq. (2), the increase of carrier density in the channel and the decrease of the scattering parameter with increasing forward body bias cause the drain current noise spectrum density to decrease considerably. Applying a body bias up to 0.5 V improves the normalized drain noise spectrum density by almost one order of magnitude. This $1/f$ noise improvement technique can be implemented in analog circuits of triple-well CMOS technologies [41].

5. Conclusions

The impact of channel carrier location and barrier height lowering on the gate and body bias dependence of low-frequency noise of surface channel n-MOSFETs is investigated. Noise calculations are made with the unified noise model by reevaluating the two important physical parameters, attenuation constant α and scattering parameter S , used in the correlated models to represent the physical phenomena, carrier tunneling and scattering. We propose that the attenuation constant is not constant but depends on the applied bias due to oxide–semiconductor barrier height lowering. We also showed that the scattering parameter depends on the average distance of carriers from the oxide–semiconductor interface that varies considerably with applied gate voltage. The low-frequency noise spectrum density is calculated using these two proposed effects. Experimental results showing the bias and geometry dependence of low-frequency noise agree with the calculated noise data to great accuracy. Furthermore, low-frequency noise improvement is observed with 0.5 V forward body bias at low gate voltage and this is explained quantitatively with the correlated noise model.

Acknowledgments

This work was carried out partly at the National Science Foundation's State/Industry/University Cooperative Research Centers' Center for Low Power Electronics (CLPE). CLPE is supported by the NSF (Grant #EEC-9523338), the State of Arizona, and Intel Corporation, Mindspeed, National Semiconductor, Raytheon and Western Design Center. We also wish to thank the anonymous reviewer for valuable comments.

References

[1] McWhorter AL. $1/f$ noise and germanium surface properties. In: Semiconductor surface physics. Philadelphia: University of Pennsylvania Press; 1957. p. 207–28.

[2] Fu HS, Sah CT. Theory and experiments on surface $1/f$ noise. IEEE Trans Electron Dev 1972;ED-19:273–85.

[3] Christensson S, Lundstrom I, Svensson C. Low-frequency noise in MOS transistors. Solid-State Electron 1968;11:797–812.

[4] Bertz F. Theory of low frequency noise in Si MOST's. Solid-State Electron 1970;13:631–47.

[5] Hooge FN. $1/f$ noise. Physica 1976;83B:14–23.

[6] Vandamme LKJ. Model for $1/f$ noise in MOS transistors biased in the linear region. Solid-State Electron 1980;23:317–23.

[7] Vandamme LKJ, de Werd HMM. $1/f$ noise model for MOSTs biased in nonohmic region. Solid-State Electron 1980;23:325–9.

[8] Hooge FN, Vandamme LKJ. Lattice scattering causes $1/f$ noise. Phys Lett 1978;66A:315–6.

[9] Jindal RP, van der Ziel A. Phonon fluctuation model for flicker noise in elemental semiconductors. J Appl Phys 1981;52:2884–8.

[10] Hung KK, Ko PK, Hu C, Cheng YC. Flicker noise characteristics of advanced MOS technologies. IEDM Tech Dig 1988:34–8.

[11] Hung KK, Ko PK, Hu C, Cheng YC. A unified model for flicker noise in metal oxide semiconductor field effect transistors. IEEE Trans Electron Dev 1990;37:654–65.

[12] Hung KK, Ko PK, Hu C, Cheng YC. A physics based MOSFET noise model for circuit simulators. IEEE Trans Electron Dev 1990;37:1323–33.

[13] Fleetwood DM. Border traps in MOS devices. IEEE Trans Nucl Sci 1992;39:269–71.

[14] Fleetwood DM, Winokur PS, Riewe LC. Effects of oxide traps, and border-traps on metal–oxide–semiconductor devices. J Appl Phys 1993;73:5058–69.

[15] Paulsen RE, White MH. Observation of near-interface oxide traps with the charge pumping technique. IEEE Electron Dev Lett 1992;13:627–9.

[16] Clevers RHM. Volume and temperature dependence of the $1/f$ noise parameter α in Si. Physica B 1989;154:214–24.

[17] Vandamme LKJ, Li X, Rigaud D. $1/f$ noise in MOS devices, mobility or number fluctuations? IEEE Trans Electron Dev 1994;41(November):1936–45.

[18] Stegherr M. Flicker noise in hot electron degraded short channel MOSFETs. Solid-State Electron 1984;27:1055–6.

[19] Li X, Vandamme LKJ. Normalized $1/f$ noise: a more sensitive diagnostic tool for hot-carrier degradation in submicron devices. In: 5th Europe Symposium on Reliability of Electron Devices Failure Physics and Analysis, Glasgow, 1994.

[20] Simoen E, Dierckes B, Claeys C. Low-frequency noise behavior of Si n-MOST's stressed at 4.2 K. IEEE Trans Electron Dev 1994;40:1296–9.

[21] Scofield JH, Fleetwood DM. Physical basis for nondestructive tests of MOS radiation hardness. IEEE Trans Nucl Sci 1991; 38:1567–77.

[22] Tsai MH, Ma TP. Effect of radiation induced interface traps on $1/f$ noise in MOSFETs. IEEE Trans Nucl Sci 1992;39:2178–85.

[23] Simoen E, Claeys C. Low-frequency noise behavior of γ -irradiated partially depleted silicon-on insulator n-channel metal-oxide–semiconductor transistors. Appl Phys Lett 1993;63:1672–4.

[24] Vandamme LKJ. $1/f$ noise in CMOS transistors. In: Ambrozy A, editor. Noise in physical systems. Budapest: Akademiai Kiado; 1990. p. 491–4.

[25] Tedja S, Williams HH, Van der Spiegel J, Newcomer FM, Van Berg R. Noise measurement results of a radiation hardened CMOS 1.2 μm p-well process. Nucl Instrum Meth Phys Res A 1992;312:579–84.

[26] Scofield JH, Borland N, Fleetwood DM. Reconciliation of different gate-voltage dependencies of $1/f$ noise in n-MOS and p-MOS transistors. IEEE Trans Electron Dev 1994;41: 1946–52.

[27] Li X, Barros C, Vandamme EP, Vandamme LKJ. Parameter extraction and $1/f$ noise in a surface and bulk-type p-channel LDD MOSFET. Solid-State Electron 1994;37:1853–62.

- [28] Brews JR. Theory of the carrier-density fluctuation in an IGFET near threshold. *J Appl Phys* 1975;46:2181–92.
- [29] Koga J, Takagi S, Toriumi A. A comprehensive study of MOSFET electron mobility in both weak and strong inversion regimes. *IEDM Tech Dig* 1994;475–8.
- [30] Mujtaba A, Takagi S, Dutton R. Accurate modeling of Coulombic scattering, and its impact on scaled MOSFETS. *Symp VLSI Tech Dig*, vol. 99, 1995. p. 99–100.
- [31] Soppa WM, Wagemann HG. Investigation and modeling of the surface mobility of MOSFETs from -25 to $+150$ °C. *IEEE Trans Electron Dev* 1988;35:970–7.
- [32] Sun SC, Plummer JD. Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces. *IEEE Trans Electron Dev* 1980;ED-27:1497–508.
- [33] Lundstrom M. *Fundamentals of carrier transport*. 2nd ed. Cambridge University Press; 1998.
- [34] Ning TH, Sah CT. Theory of scattering of electrons in a nondegenerate semiconductor surface inversion layer by surface oxide charges. *Phys Rev B* 1972;6:4605–13.
- [35] Sah CT, Ning TH, Tschopp LL. The scattering of electrons by surface oxide charges and by lattice vibrations at the silicon-silicon dioxide interface. *Surf Sci* 1972;32:561–75.
- [36] Stern F. Self consistent results for n-type Si inversion layers. *Phys Rev B* 1972;5:4891–9.
- [37] Ohkura Y. Quantum effects in Si n-MOS inversion layer at high substrate concentration. *Solid-State Electron* 1990;33:1581–85.
- [38] Nicollian EH, Brews JR. *MOS metal oxide semiconductor physics and technology*. New York: Wiley; 1982.
- [39] McLean FB, Boesch HE. *IEEE Trans Nucl Sci* 1989;36:1772–83.
- [40] Sze SM. *Physics of semiconductor devices*. 2nd ed. New York: Wiley; 1993.
- [41] Muth W. Matrix method for latch-up free demonstration in a triple-well bulk-silicon technology. *IEEE Trans Nucl Sci* 1992; 39(part I):396–400.
- [42] Taur Y, Ning TH. *Fundamentals of modern VLSI devices*. Cambridge University Press; 1998.