Charge-Coupled Devices

Surface Potential
Charge Transfer
Charge Input / Output
Charge Transfer Efficiency
Surface Potential

- $V_D = 0 \quad V_G = 0$
- $V_D = 0 \quad V_G = 5 \text{ V}$
- $V_D = 5 \text{ V} \quad V_G = 5 \text{ V}$
- $V_D = 5 \text{ V} \quad V_G = 8 \text{ V}$

- Channel
- No Channel
- $\phi_s \sim 2\phi_F$
- $\phi_s < V_G$
- $\phi_s \sim 2\phi_F + V_D$

© D.K. Schroder, Semiconductor Device Theory - 2
Surface Potential

- Surface potential depends on:
  - Gate voltage
  - Flatband voltage
  - Doping density
  - Oxide thickness
  - Inversion charge density

\[ V_G = V_{FB} + V_{ox} + \phi_s \]

\[ V_{ox} = -\frac{Q_s}{C_{ox}} = -\frac{Q_n + Q_b}{C_{ox}} \]

\[ Q_b = -qN_A W; \quad Q_n < 0 \]

\[ \phi_s = V' - V_o \left( \sqrt{1 + \frac{2V'}{V_o}} - 1 \right) \]

\[ V' = V_G - V_{FB} + \frac{Q_n}{C_{ox}} \]

\[ V_o = \frac{qK_s \varepsilon_o N_A}{C_{ox}^2} \]

Thermally generated electrons flow to ground
MOS Capacitor

- Figure (a) shows a MOS capacitor with a $p$-type semiconductor and an initial charge $Q_N$.
- Figure (b) illustrates the electric field $E$ and the Fermi levels $F_P$ and $F_N$.
- Figure (c) depicts the electric field $E$ and the potential $q\phi_{s0}$, $q\phi_{s1}$, and $q\phi_{s2}$.

© D.K. Schroder, Semiconductor Device Theory - 2
**CCD Charge**

- Charge is confined to the potential well

![Diagram showing CCD Charge with potential wells labeled $\phi_s = 2\phi_F$, $\phi_{s1}$, $\phi_{s2}$, $\phi_{s3}$, and $V_{G1}$ in the x-axis and E in the y-axis.](image)
Charge Confinement

- Charge must be confined in the \(x\), \(y\), and \(z\) directions.

- One way to confine in the \(x\) direction is with gate voltages.

\[ \phi_s = V'_G + \frac{Q_n}{C_{ox}} - V_0 \left[ \sqrt{1 + \frac{2(V'_G + Q_n / C_{ox})}{V_0}} - 1 \right] \]

- Maximum charge density without spilling into adjacent wells is

\[ Q_{n,m} = -C_{ox}(V_{G2} - V_{G1}) \]
**Charge Confinement**

- **x direction**
  - Charge confined by gate voltage

- **y direction**
  - Charge confined by oxide thickness
Charge Input

- Diode reverse biased
- Input voltage applied between $G_1$ and $G_2$
- Diode briefly zero biased and charge spills into $G_2$ potential well
- Diode reverse biased and excess charge spills into diode

\[
\phi_s = V' + \frac{Q_n}{C_{ox}} - V_0 \left[ \sqrt{1 + \frac{2(V' + Q_n / C_{ox})}{V_0}} - 1 \right]
\]

- Surface potential under gates $G_1$ and $G_2$ is equal, giving

\[
Q_n = -C_{ox} (V_{G2} - V_{G1}) = -C_{ox} V_i
\]
Signal charge routed into floating source

$V_S$ detected with high input impedance MOSFET

$\Delta V_{out} = Q_n / C$
Three-Phase Charge Transfer

- At any time there is a barrier between charge packets so the charge packets do not mix
- Gate voltage $\Rightarrow$ charge transfer

\[ V_{G1} \quad \phi_1 \quad V_{G2} \quad \phi_2 \quad V_{G1} \quad \phi_3 \]

\[ t=t_1 \quad t=t_2 \quad t=t_3 \quad t=t_4 \]
4-Phase, 2-Phase Charge Transfer

- Four-phase: need four waveforms
- Two-phase: need asymmetry
  - Different oxide thickness
  - Implanted acceptor ions
Charge Transfer Efficiency

- Charge transfer inefficiency per elemental transfer $\varepsilon$
  - Fraction of charge left behind when charge is transferred from one well to the next
  - $n =$ number of elemental transfers
  - $P =$ number of clocking phases
  - $N =$ number of stage transfers
  - $\alpha =$ charge transfer inefficiency per stage
  - $n = PN$ and $\alpha = P\varepsilon$

- After $N$ transfers, charge is no longer localized in one well, but is spread out over several trailing wells

\[
D_{i,N} = \frac{Q_i}{Q} = \frac{[N!(1-\alpha)^i\alpha^{N-i}]}{[(N-i)!i!]} 
\]

- After $N$ stage transfers

\[
\text{Deficit} = 1 - D_{N,N} = 1 - (1 - \alpha)^N \\
= 1 - (1 - P\varepsilon)^{n/P} \approx N\alpha = n\varepsilon
\]
Charge Transfer

- Self induced drift
  ⇒ fringing field
  ⇒ diffusion
- Charge left behind mixes with following charge packet

\[
\begin{align*}
Q_i &= 1 & N = 0 \\
Q_i &= 1 - \alpha & N = 1 \\
Q_i &= \alpha^2 2\alpha(1-\alpha) & N = 2
\end{align*}
\]
Interface State Trapping

- Interface state trapping important charge transfer inefficiency mechanism
- When charge packet enters potential well, electrons are captured by interface states
- Capture is relatively independent of energy and very fast

\[ \tau_c = \frac{1}{\sigma_n v_{th} n_s} \]

\[ \tau_c = 10^{-10} \quad s : n_s = 10^{18} \text{ cm}^{-3} \]

\[ \sigma_n = 10^{-15} \text{ cm}^2; v_{th} = 10^7 \text{ cm / s} \]
Interface State Trapping

- When charge packet leaves potential well, some electrons are emitted by interface states
- Emission is dependent on energy
- Charge transfer efficiency improved by bias charge (fat zero)
  - Small amount of charge always in potential wells

\[
\tau_e = \frac{\exp(\Delta E / kT)}{\sigma_n v_{th} N_c} = 10^{-11} \exp(\Delta E / kT)
\]

\[
N_c = 10^{19} \text{ cm}^{-3}; \quad \sigma_n = 10^{-15} \text{ cm}^2
\]

\[
v_{th} = 10^7 \text{ cm/s}
\]
Bulk Channel CCD

- Charge is transferred in the $n$-semiconductor, not at the surface.
- No interaction with interface states \( \Rightarrow \) higher transfer efficiency.

\[
\begin{align*}
\phi_1 & \quad \phi_2 \quad \phi_3 \\
0 & \quad V_n \\
p & \quad n^+ \\
p & \quad n
\end{align*}
\]

Signal charge packet

\[
\begin{align*}
V_G & \quad n \\
V_G & \quad p
\end{align*}
\]
Bulk Channel CCD

- When the well fills, the charge moves towards the surface
- Leads to interaction with interface states

[Diagram of Bulk Channel CCD with labels and equations]
Review Questions

- What happens to the surface potential as a function of time after an MOS-C is driven into deep depletion?
- How is charge confined in the x and y-direction?
- How are charge input and output implemented?
- What affects charge transfer?
- Why is charge transfer important?
- How can charge transfer efficiency be improved?
- What three mechanisms determine charge transfer?
- How does a bulk CCD differ from a surface CCD?