Power Considerations

Power Dissipation
Active Versus Passive Power
“On” and “Off” Currents
High-\(\kappa\) Dielectrics
Low-\(\kappa\) Dielectrics
Power Dissipation in RC Circuit

\[ V_o = V_1 \left(1 - e^{-t/RC}\right) \]

\[ i(t) = C \frac{dV_o}{dt} = \frac{V_1 - V_o}{R} = \frac{V_1}{R} e^{-t/RC} \]

\[ P = \int_0^\infty i(t)^2 R dt = \frac{V_1^2}{R} \int_0^\infty e^{-2t/RC} dt = \frac{CV_1^2}{2} \]

Independent of R!

Energy in C = \[ \int_0^{V_1} Q dV_o = \int_0^{V_1} CV_o dV_o = \frac{CV_1^2}{2} \]

Energy in supply = \[ \int_0^\infty V_1 i(t) dt = \frac{1}{R} \int_0^\infty V_1^2 e^{-t/RC} dt = CV_1^2 \]
CMOS Power Dissipation

- Replace transistor by resistor and switch
- Energy in one cycle
  - Charging $0 \Rightarrow 1$
    - $CV^2$ from power supply
    - $CV^2/2$ dissipated in $R$
    - $CV^2/2$ stored on $C$
  - Discharging $1 \Rightarrow 0$
    - Power supply does nothing
    - $CV^2/2$ dissipated in $R$
    - $C$ has no energy
- Total “dissipated” $CV^2$
- Dissipated power: $fCV^2$
CMOS Power Dissipation

- Power dissipation sources:
  \[ P = P_{\text{switch}} + P_{sc} + P_{off} + P_G \]
  \[ P_{\text{switch}} = \alpha f C V_{DD}^2; \quad P_{sc} = I_{sc} V_{DD}; \]
  \[ P_{off} = I_{off} V_{DD}; \quad P_G = I_G V_{DD} \]

\(\alpha\): switching activity; \(I_{sc}\): short circuit path when n and p-channel MOSFETs are “on”
\(I_{off}\): drain leakage current and subthreshold leakage current when device is “off”
\(I_G\): gate leakage current

- Reduce power by reducing
  - Supply voltage \(V_{DD}\) \(\downarrow\); need to reduce \(V_T\) to maintain drive current
  - Capacitance \(C\)
  - Off current \(I_{off}\) - increase \(V_T\)
  - Frequency \(f\) \(\downarrow\); parallel architectures

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"On" – "Off" Current

- **Subthreshold**
  - Subthreshold slope = $m$; Subthreshold swing $S = 1/m$

\[ I_D = I_T e^{q(V_G-V_T)/nkT} \]
\[ I_{off}(V_G = 0) = I_T e^{-qV_T/nkT} \]

\[ S = \frac{dV_G}{d[\log(I_D)]} = 2.3nkT/q \]
\[ = 60n(T/300) \text{ mV/decade of } I_D \]

- **Above threshold**

\[ I_{Dsat} = I_{on} = \frac{W\mu_{eff}C_ox}{2L} (V_G - V_T)^2 \]

Want $I_{on}$ high, $I_{off}$ low!
“On” Current

- **W/L ~ constant**
- **$\mu_{eff} \downarrow$**
  - Reduced drive current
- **$V_G \downarrow$**
  - Reduced electric field
  - Reduced power
  - Reduced drive current
  - Increased delay time
- **$V_T \downarrow$**
  - Increased drive current
  - Increased “off” current

$$I_{on} = \frac{W}{2L} \mu_{eff} C_{ox} (V_G - V_T)^2$$

- **$(V_G-V_T) \downarrow$**
  - Reduced drive current
- **$C_{ox} \uparrow$ since $t_{ox} \downarrow$**
  - Increased drive current
  - Oxide leakage current
  - Boron penetration

*I_{on} should not decrease!*

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Threshold and Supply Voltages

- How has $V_T$ changed with $V_{DD}$? Less than called for by scaling rules
- $V_{DD} - V_T$ is continually decreasing
The “off” current is due to subthreshold, punchtough, gate-induced drain leakage, drain junction leakage, and oxide currents.

$I_{off}$ should not increase!
**Dynamic \( V_T \) Control**

- Forward bias \( V_{SB} < 0 \):
  - At \( V_G = 0 \), threshold voltage is high ⇒ low “off” current
  - At \( V_G > 0 \), threshold voltage is low ⇒ high “on” current

\[
V_T = V_{FB} + 2\phi_F + \gamma \sqrt{2\phi_F - V_{SB}}
\]

\( V_T \)↓ with forward-biased S/B junction!

![Graph showing current vs. voltage for different conditions](image)

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Propagated Delay Time

- Conflicting design requirements between reducing $V_{DD}$, $V_T$, $I_{leak}$, $C$, and increasing performance
- The propagation delay time is $t_d = \frac{C\Delta V}{I}$

$$t_d = \frac{CV_{DD}}{I_D}$$
$$= \frac{2LC}{W\mu_{eff}C_{ox}V_{DD}(1-V_T/V_{DD})^2}$$
$$= \frac{K}{C_{ox}V_{DD}(1-V_T/V_{DD})^2}$$

For low $t_d$ want high $V_{DD}$, low $V_T$

Design space is shrinking!
Low - K Dielectrics

- Propagation delay along interconnects requires reduced $K_{ox}$
- Ideally $K = 1$ (air)
- Practically $K < 3.5$

$$\tau = RC = \frac{\rho L}{Wt} \frac{K_{ox} \varepsilon_0 LW}{t_{ox}} = \frac{\rho K_{ox} \varepsilon_0 L^2}{tt_{ox}}$$

Need low $\rho$ and low $K_{ox}$
Low-K Dielectrics

- Low-K dielectrics reduce wiring capacitance ⇒ reduce power
  \[ P = \alpha C f V^2 \]

- Low-K dielectrics tend to be “fluffy”
- To reduce the dielectric constant, introduce air pockets into the material
  - Dielectric constant
  - Hardness
  - Adhesion
  - Thermal expansion
  - Process compatibility
  - Swelling
## Low – K Dielectrics

<table>
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<th>$K$ Value</th>
<th>Organic Polymers</th>
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<td>$\text{Xerogel}$</td>
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Propagation delay depends on metal conductivity and interlevel dielectric constant.

- Al: $\rho = 3 \, \mu\Omega\cdot\text{cm}$
- Cu: $\rho = 1.7 \, \mu\Omega\cdot\text{cm}$
- SiO$_2$: $K_{ox} = 4$
- Low K: $K_{ox} = 2$
- Al/Cu: 0.8 $\mu$m thick
- Al/Cu: 43 $\mu$m long

Ultimate Low - $K$

- $K \approx 1.9$
- Apply and heat liquid copolymer
- Assembles into two-dimensional layer
- Ion bombardment forms it into long tunnels
- Acid flush leaves clean cavities
Why do we need high-$K$ dielectrics?

\[ I_D = \frac{W\mu_{\text{eff}}C_{\text{ox}}}{L} (V_G - V_T)^2 = \frac{W\mu_{\text{eff}}K_{\text{ox}}\varepsilon_o}{L t_{\text{ox}}} (V_G - V_T)^2 \]

With scaling
- $W$ and $L$ decrease same amount
- $\mu_{\text{eff}}$ remains about the same or decreases
- $(V_G - V_T)$ decreases

To keep drain current constant
- $t_{\text{ox}}$ decreases – oxide leakage current increases
- $K_{\text{ox}}$ increases – thicker insulator, reduced oxide leakage current
**High-K Dielectrics**

- The dielectric constant, band gap and dielectric/Si barrier height are important.
- Tunneling probability
  \[ T = \exp\left(-2t_{ox}\sqrt{\frac{2qm^*\phi_B}{\hbar^2}}\right) \]
- Need
  - High dielectric constant
  - High band gap
  - Low leakage current
  - Thermodynamic stability
  - Low flatband voltage shift
  - Good reliability
  - Good insulator/Si interface quality
  - High insulator/Si interface barrier
  - Process compatibility

**High - K Dielectrics**

There is a trade off between:
- Dielectric constant
- Band gap
- Oxide/Si barrier height
- Breakdown voltage

HfO$_2$ based dielectrics used in advanced devices

High - K Dielectrics

- Problems
  - Low band gap
  - Low barrier height
  - Low breakdown electric field
  - Poor insulator/Si interface
    - Thin intervening SiO₂ layer
  - Oxide charge
  - Low electron/hole mobility
    - Strained Si

- MOS process compatible?

Review Questions

- What determines CMOS power dissipation?
- What are “on” and “off” currents
- What determines propagation delay time?
- Why do we need low-\(K\) dielectrics?
- Why do we need high-\(K\) dielectrics?
- What are the conflicting demands of high \(on\) current and low \(off\) current?
- What are the conflicting demands of CMOS power dissipation and propagation delay time?